

FIG. 1

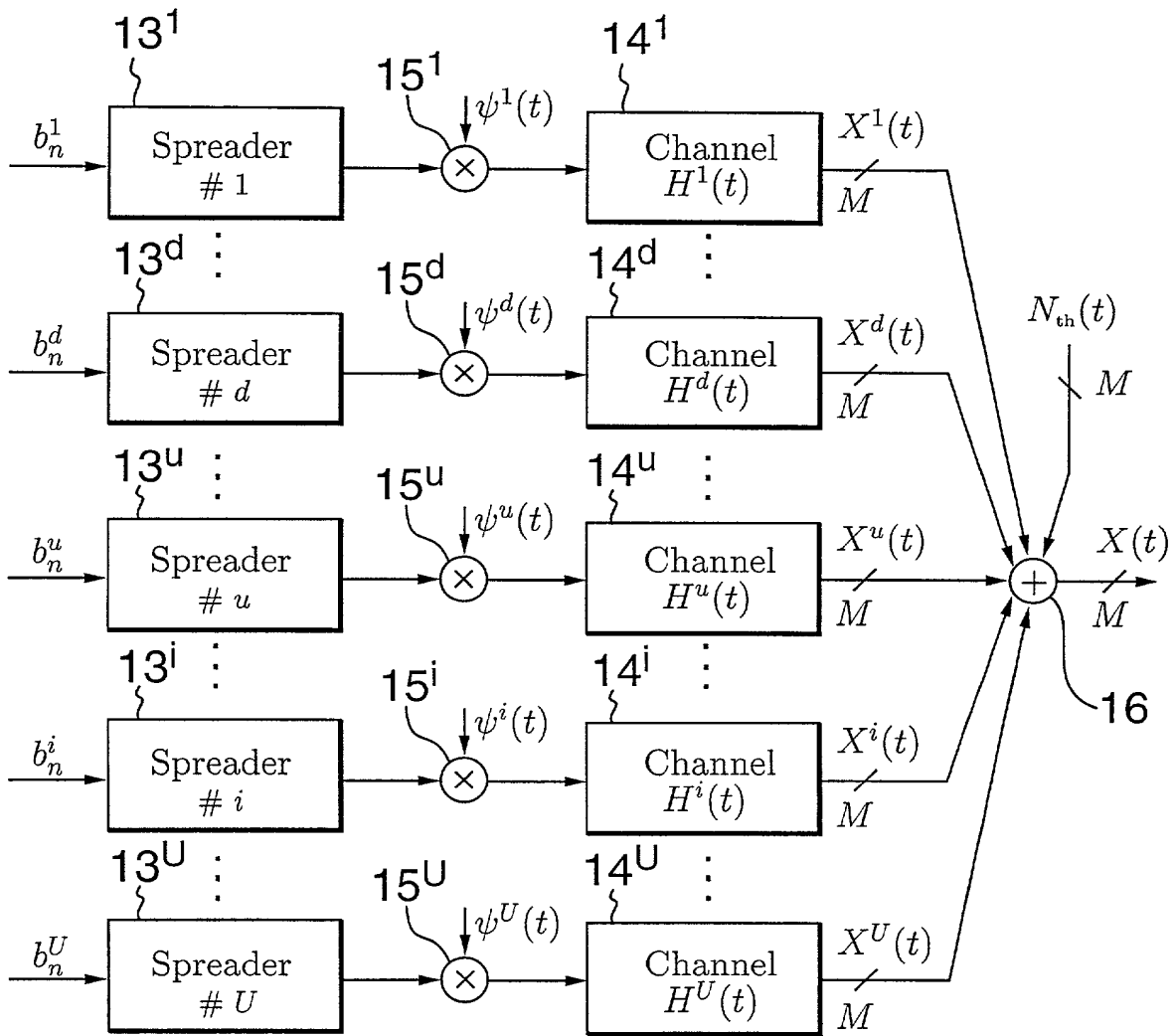


FIG. 2

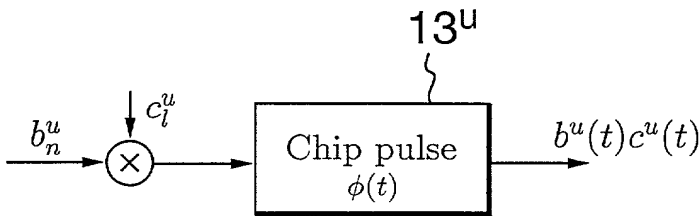


FIG. 3

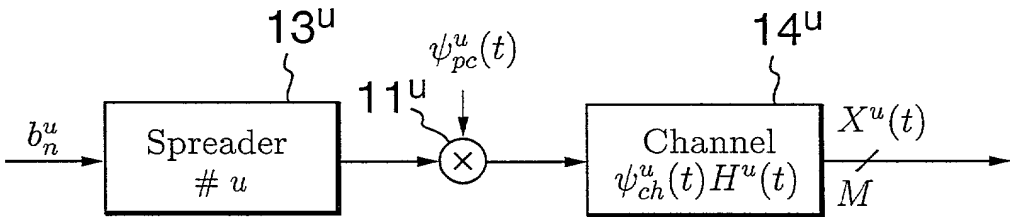


FIG. 4(a) \equiv

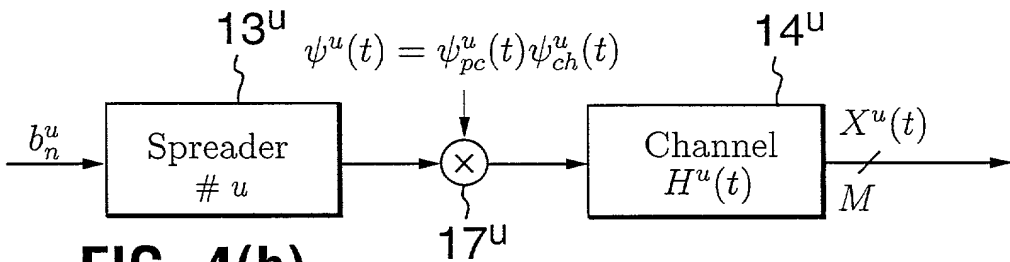


FIG. 4(b)

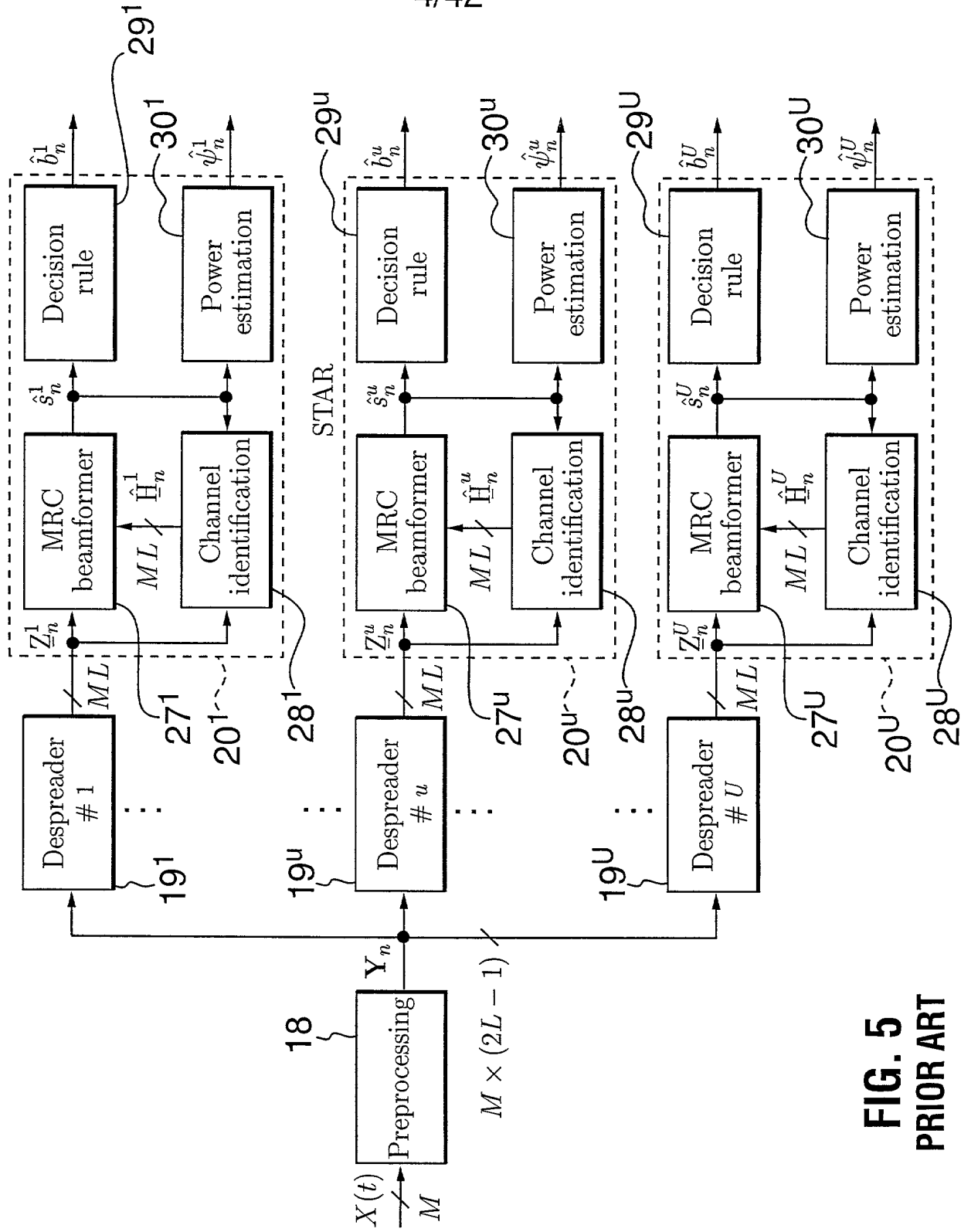
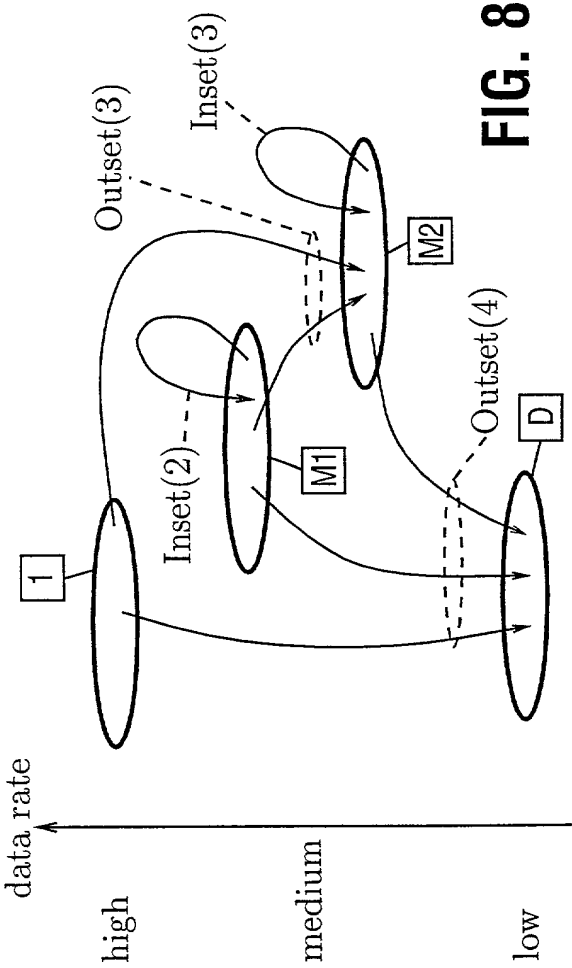
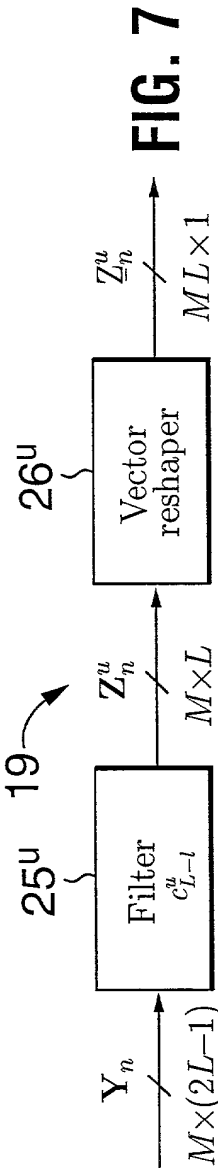
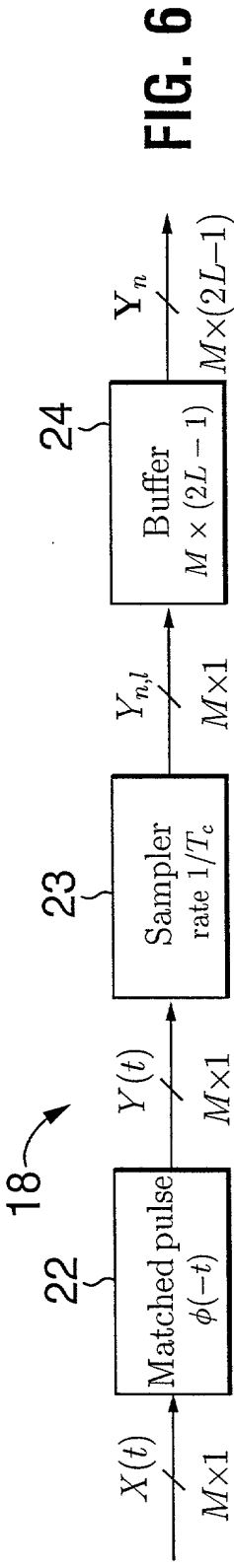


FIG. 5
PRIOR ART



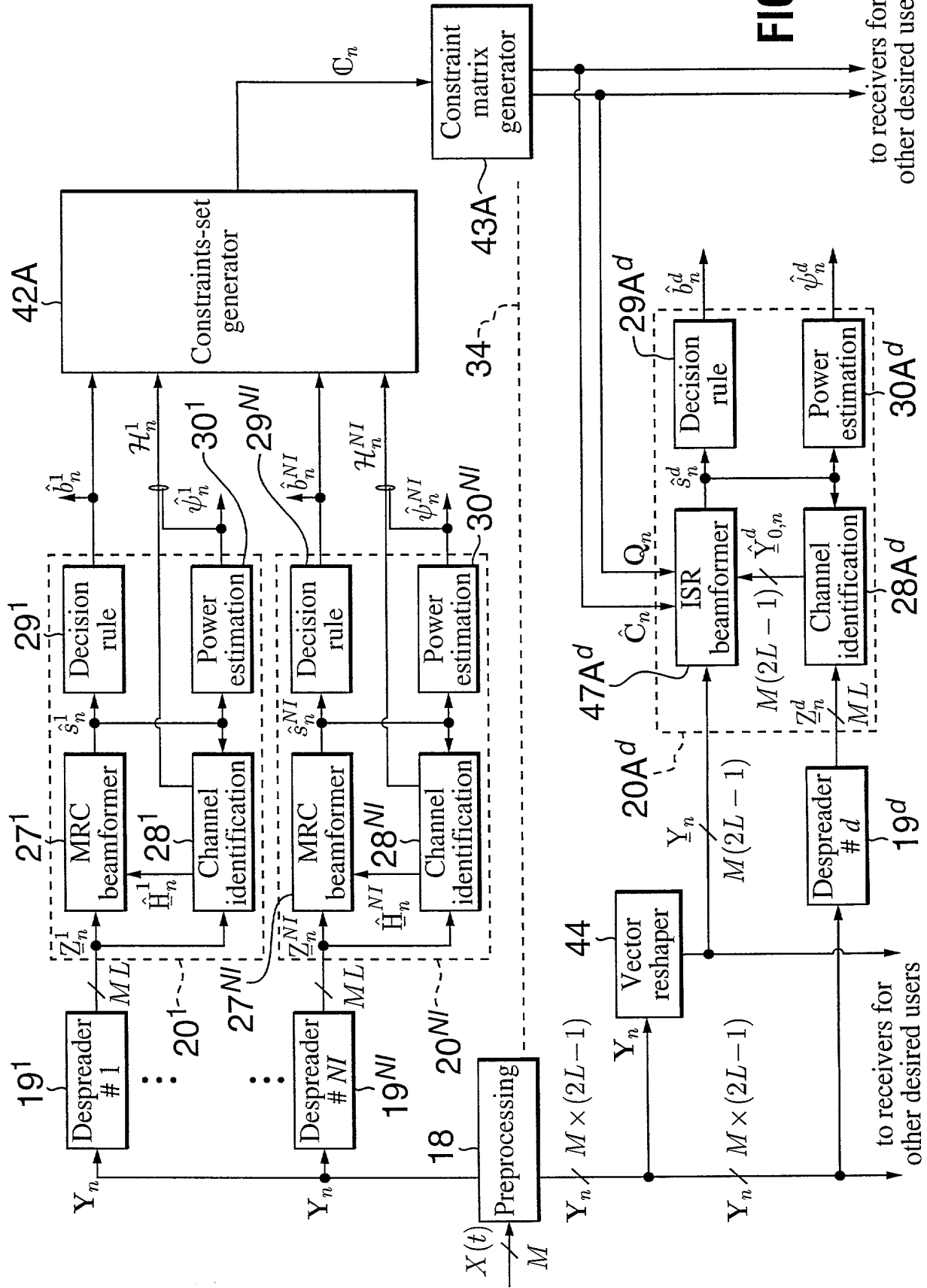


FIG. 9

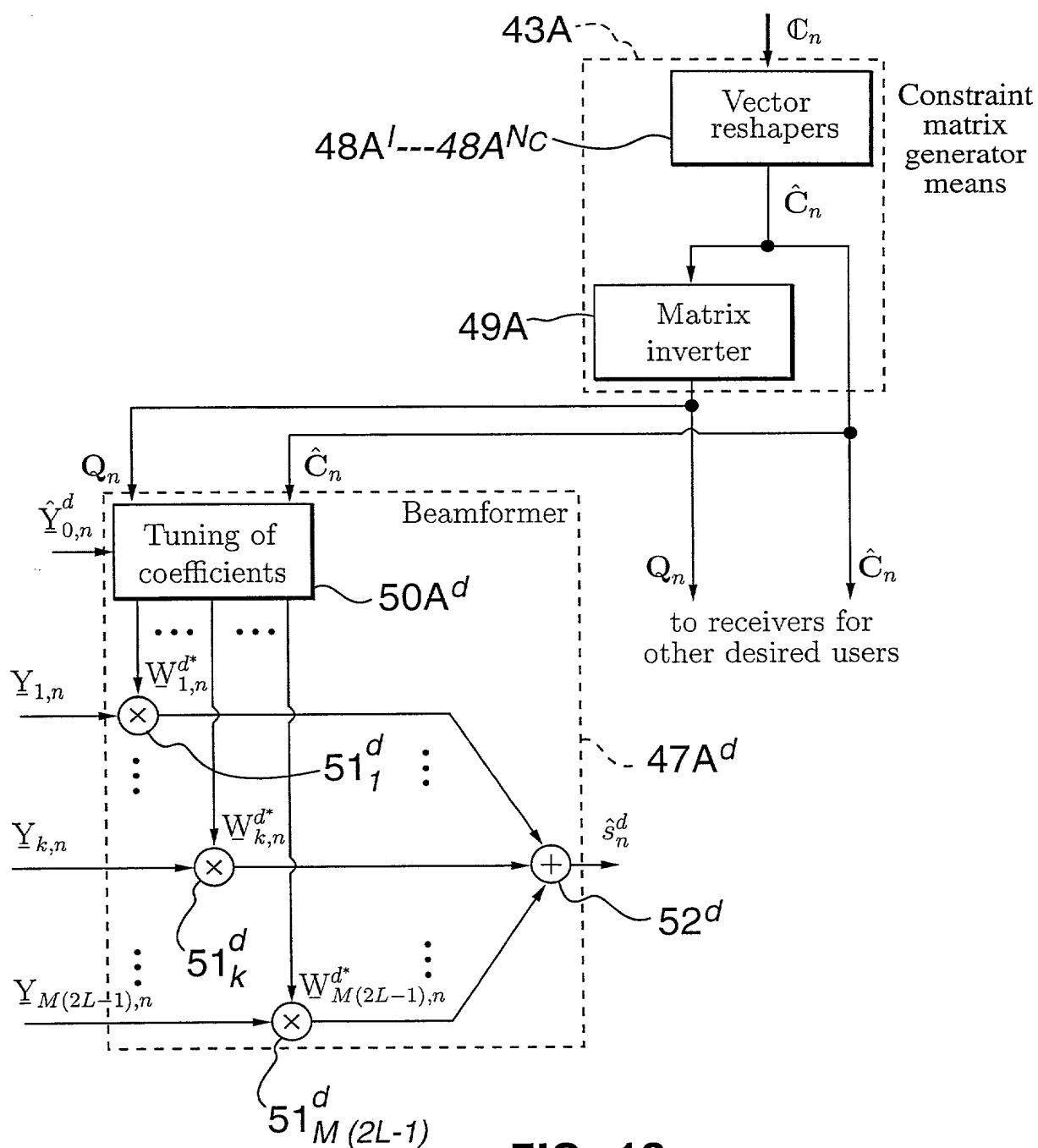


FIG. 10

FIG. 1 is a block diagram of a multiuser detection system. The system processes multiple users' signals. User signals Y_n are despread by despreaders #1 to #NI (19¹ to 19^{NI}). The resulting signals Z_n^1 to Z_n^{NI} are then processed by MRC beamformers (27¹ to 27^{NI}) and channel identification blocks (28¹ to 28^{NI}). The outputs are fed into decision rules (29¹ to 29^{NI}) and power estimation blocks (30¹ to 30^{NI}). The decision rules output H_n^1 to H_n^{NI} , and the power estimation blocks output b_n^1 to b_n^{NI} and ψ_n^1 to ψ_n^{NI} . These are fed into a constraints-set generator (42B), which also receives C_n . The constraints-set generator outputs constraints to a constraint matrix generator (43B). The constraint matrix generator outputs a matrix to the despreaders (19^d) for other users. The despreaders output Y_n to the MRC beamformers (27^d) and channel identification blocks (28^d). The MRC beamformers output Z_n^d to the decision rules (29^d) and power estimation blocks (30^d). The decision rules output b_n^d , and the power estimation blocks output ψ_n^d . The system also includes a preprocessing block (18) and a channel identification block (20B^d).

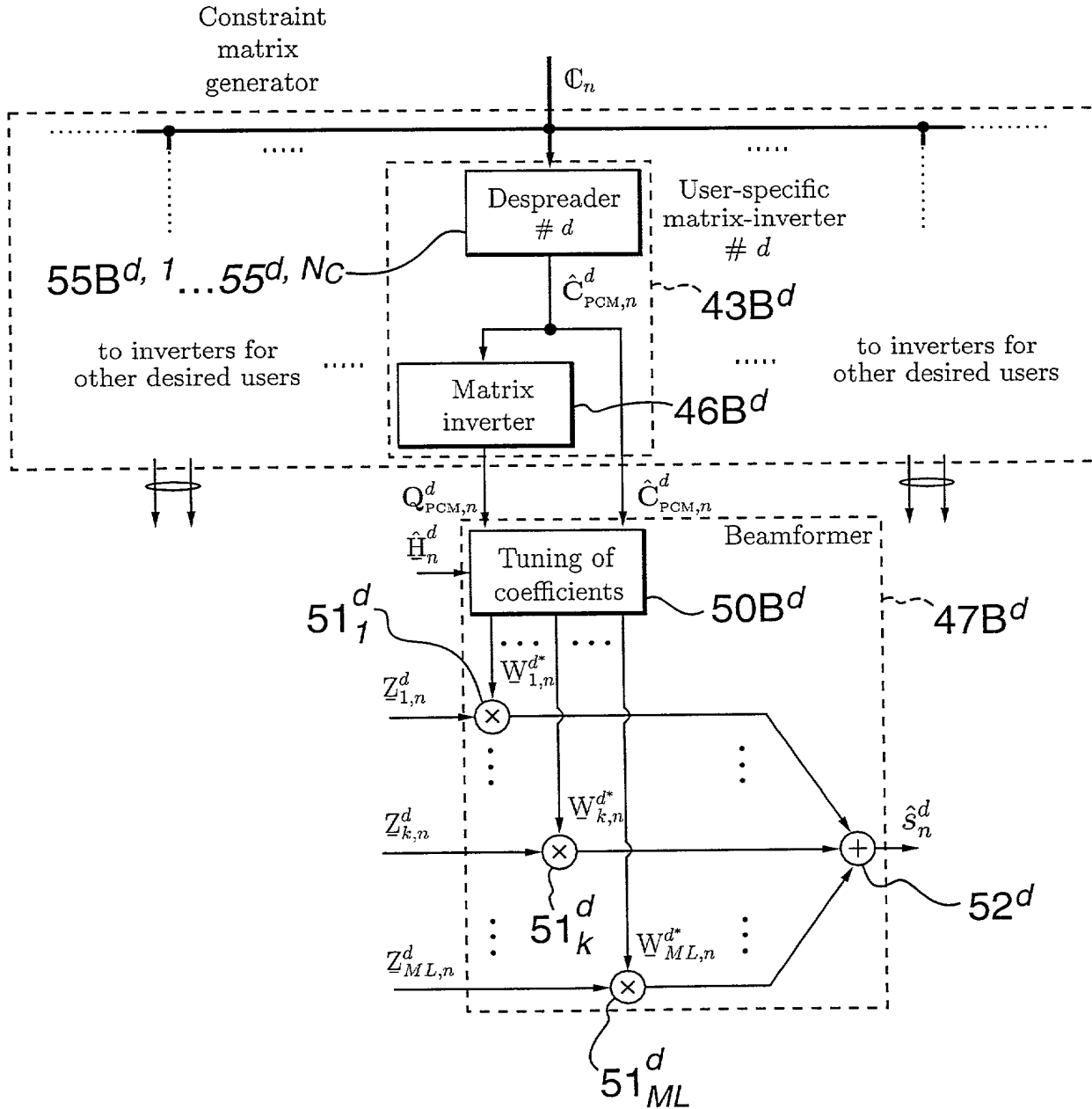


FIG. 12

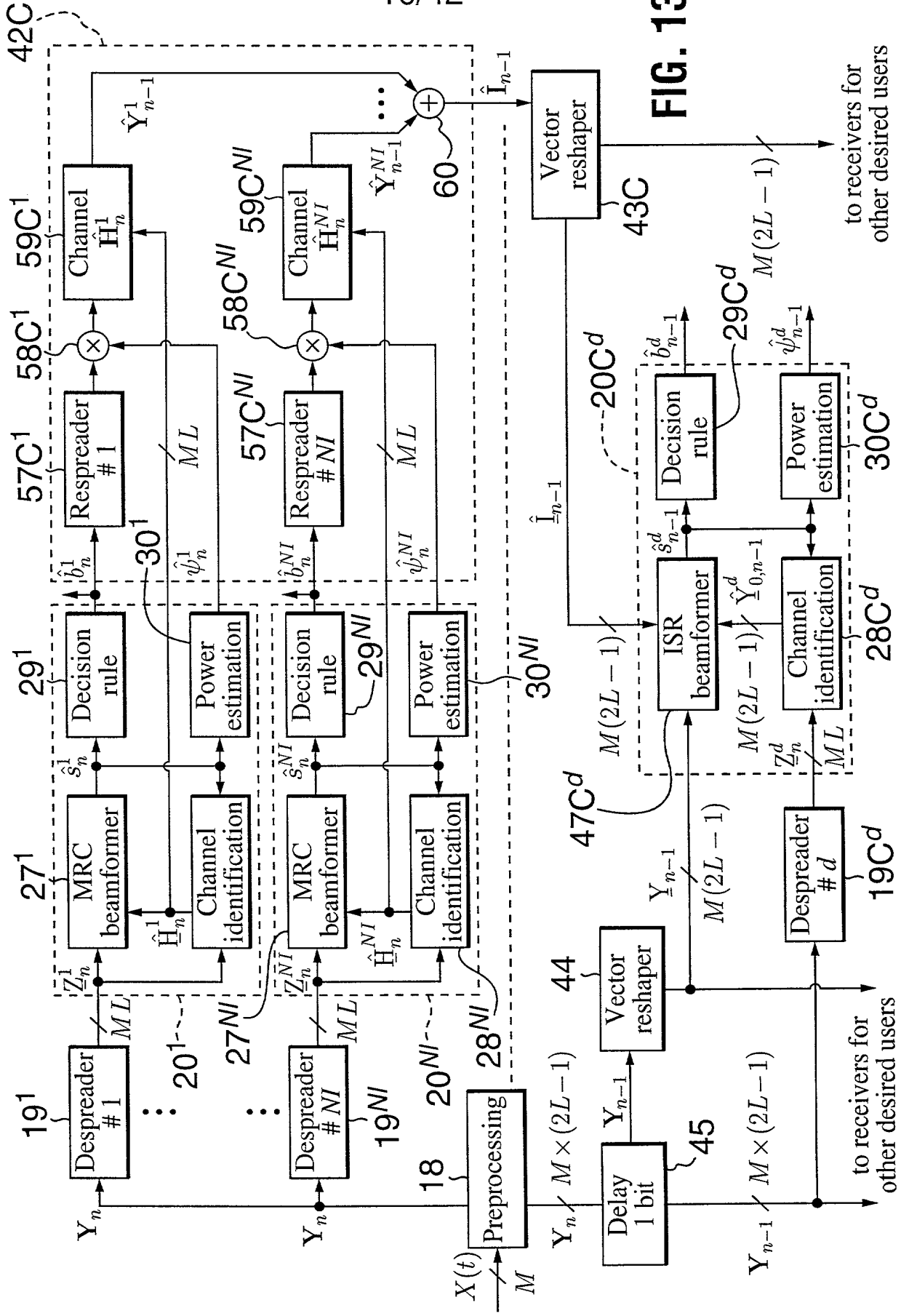


FIG. 13

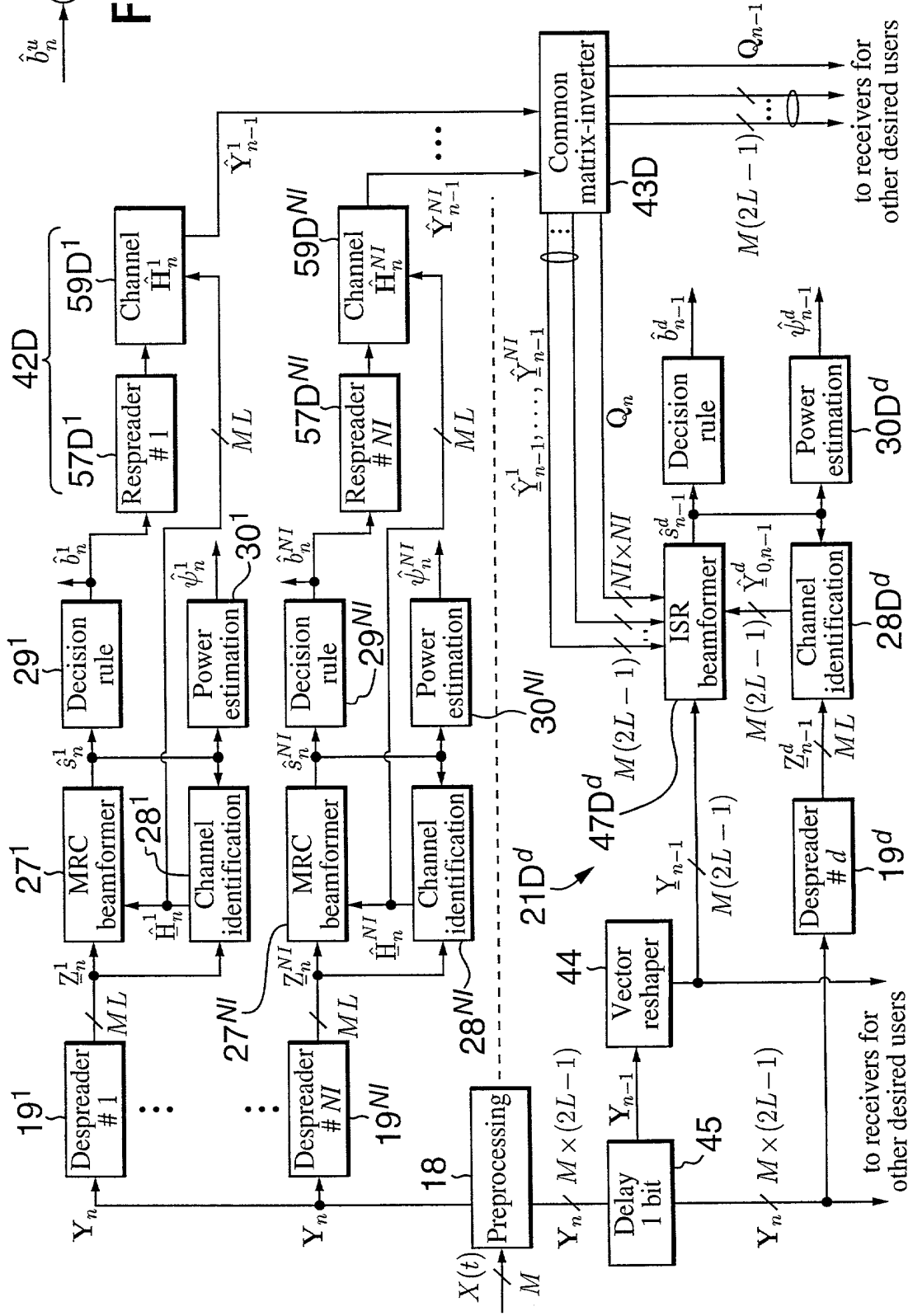
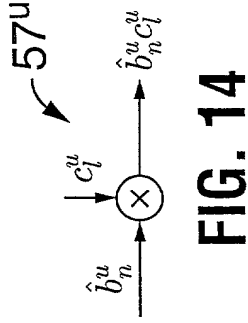
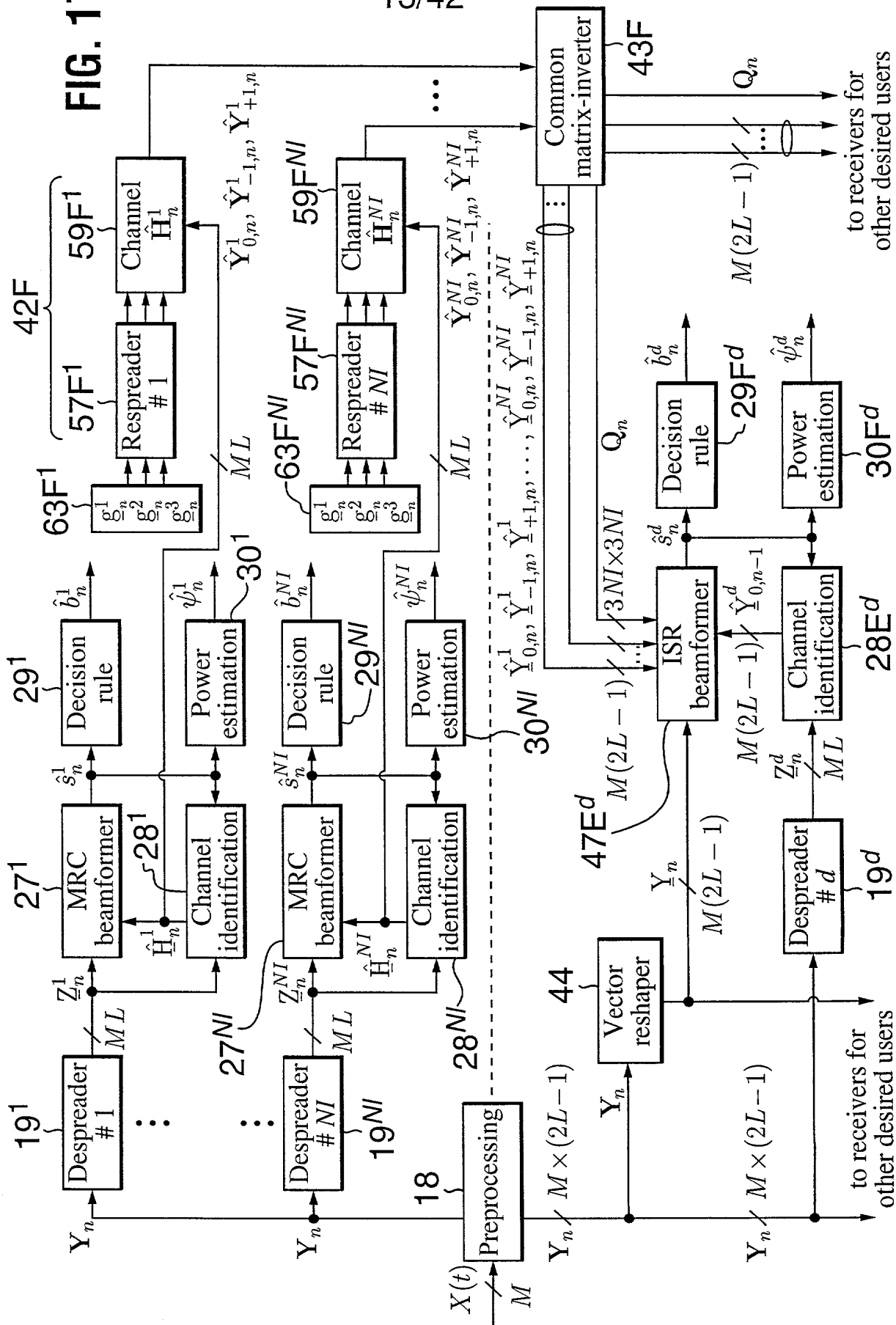


FIG. 1

The diagram illustrates a multi-user MIMO system architecture. The system consists of N_f users, each represented by a block labeled 19^1 to 19^{N_f} . Each user's received signal Y_n is processed by a despreaders (28E¹ to 28E^{N_f}), followed by a vector resaper (44) and a delay (45). The signals are then processed by a common matrix-inverter (43E) which outputs signals to receivers for other desired users. The system also includes a power estimation and decision rule (29¹ to 29^{N_f}) and a channel identification (28E¹ to 28E^{N_f}) block. The signals are then processed by a common matrix-inverter (43E) which outputs signals to receivers for other desired users.

FIG. 17



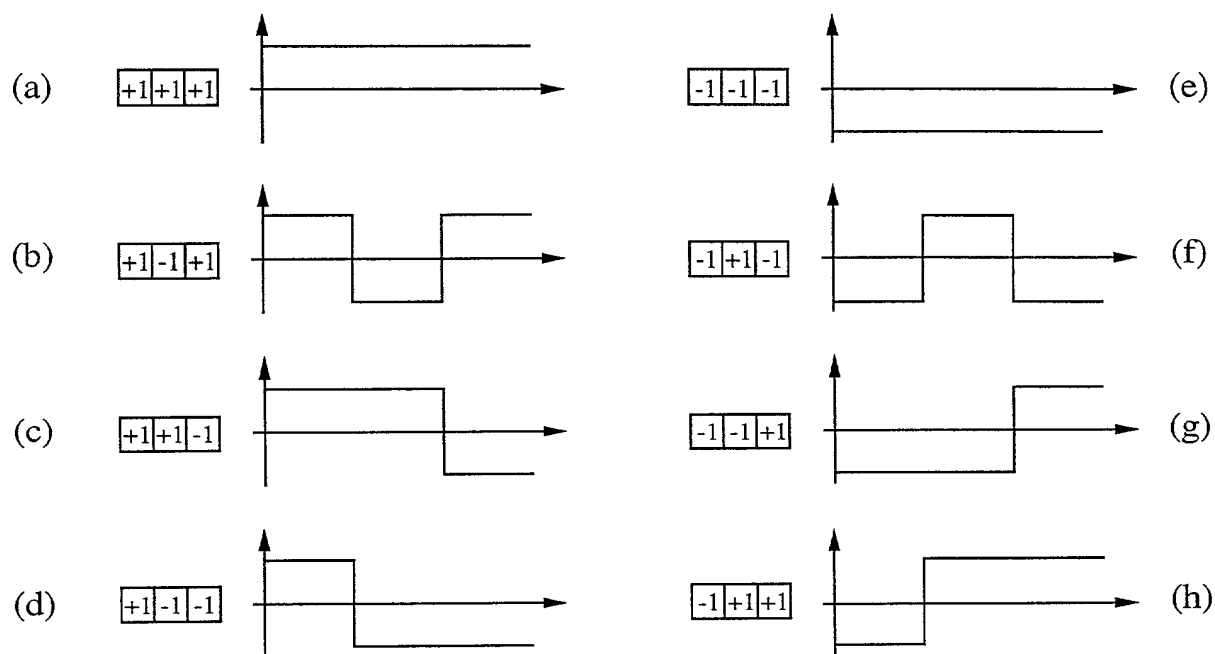


FIG. 18

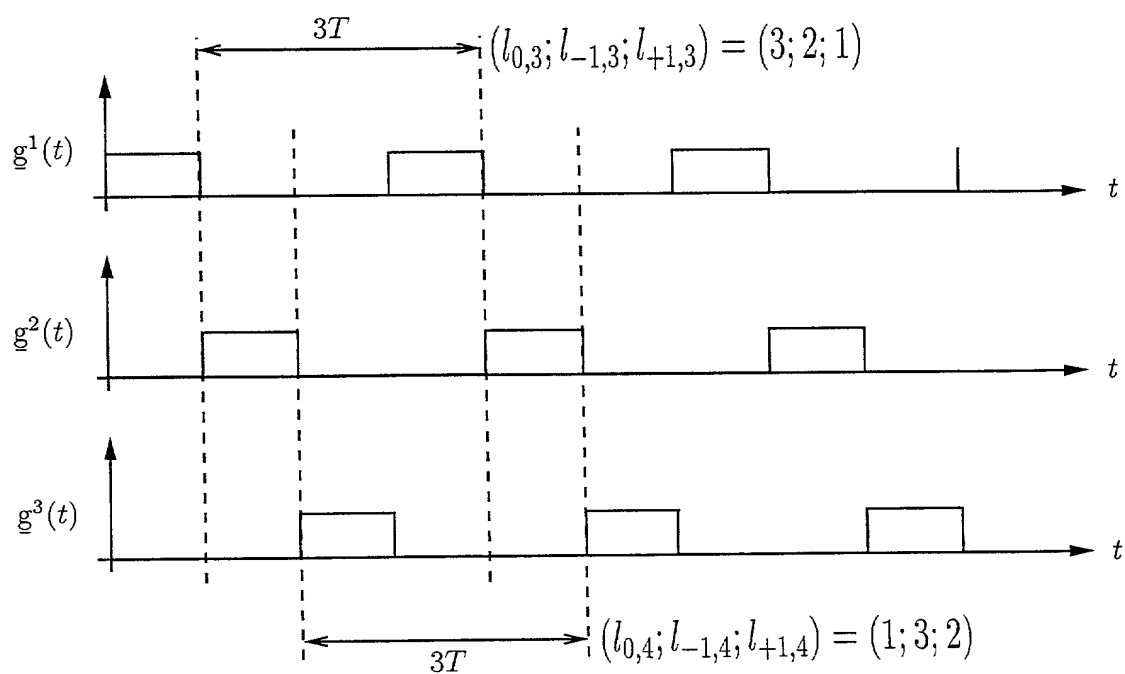


FIG. 19

FIG. 20

15/42

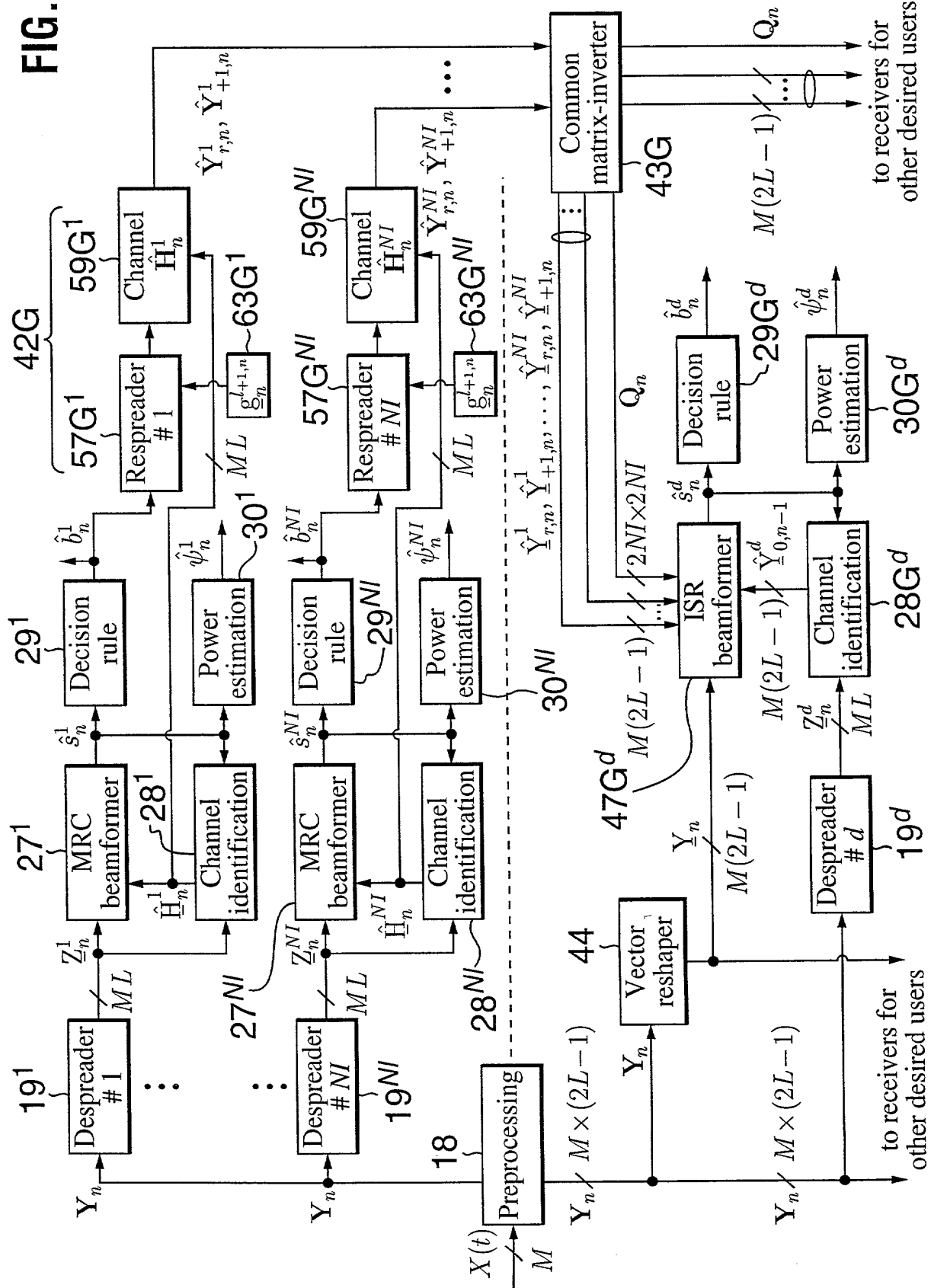


FIG. 21

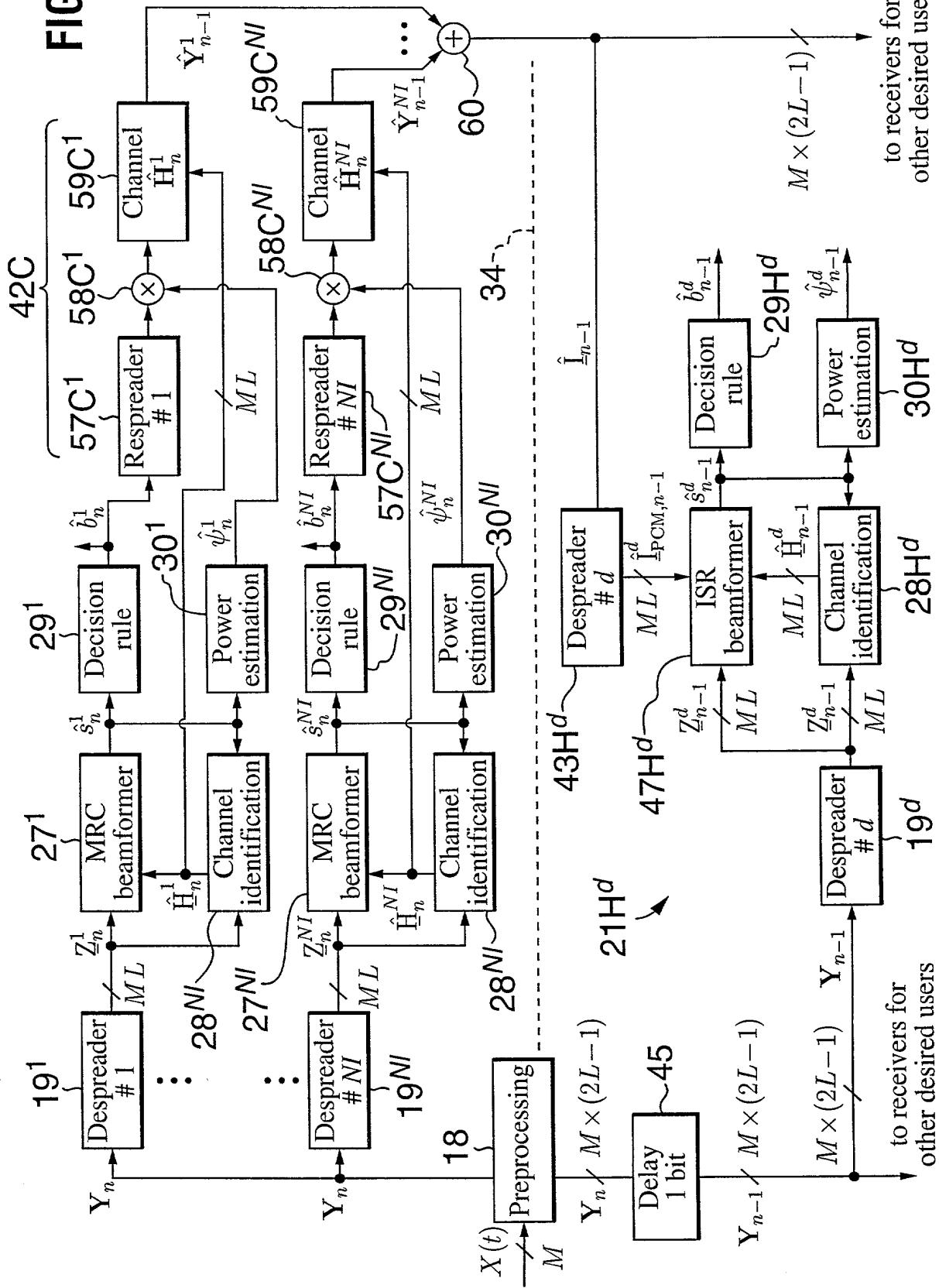


FIG. 22

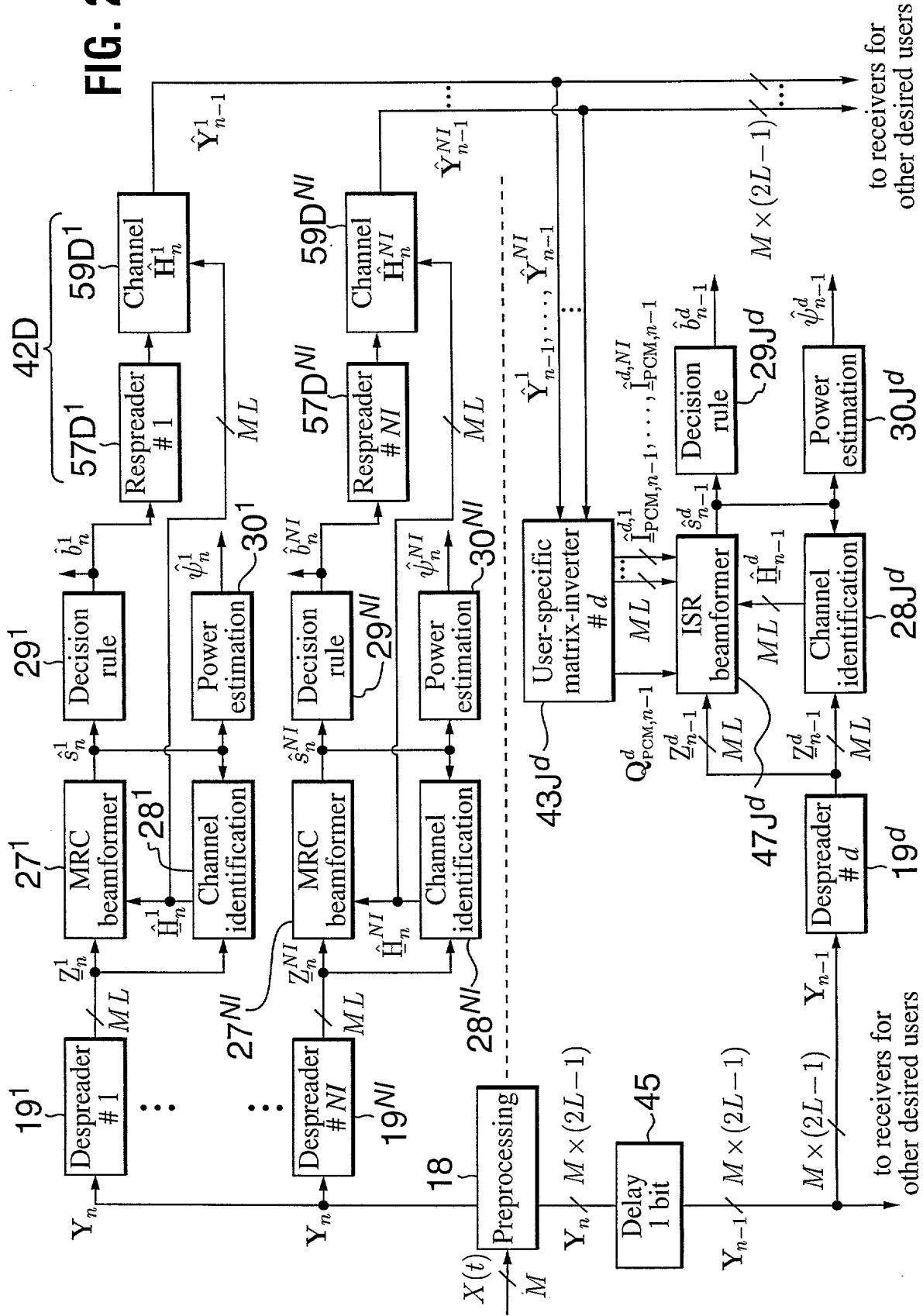


FIG. 23

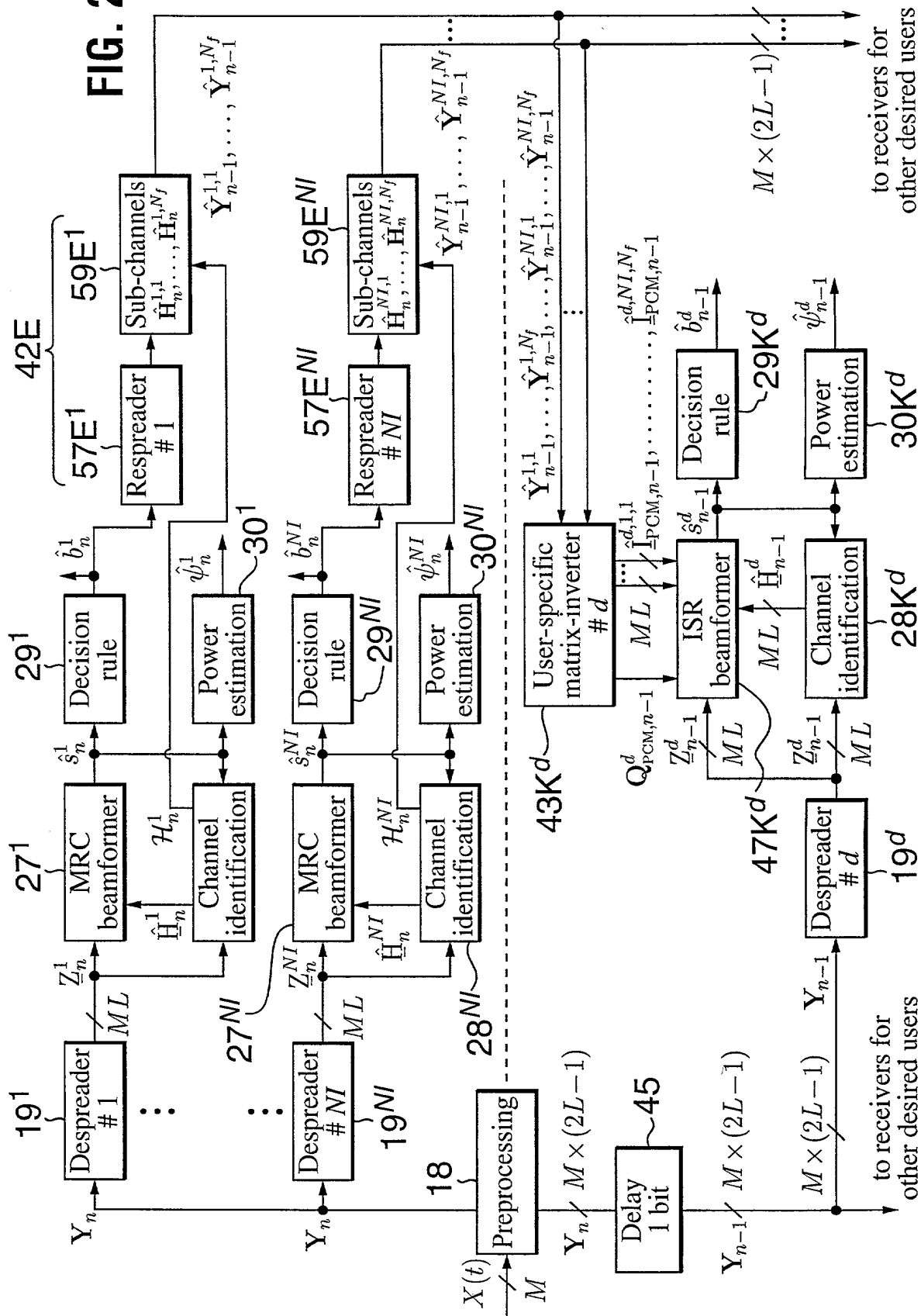
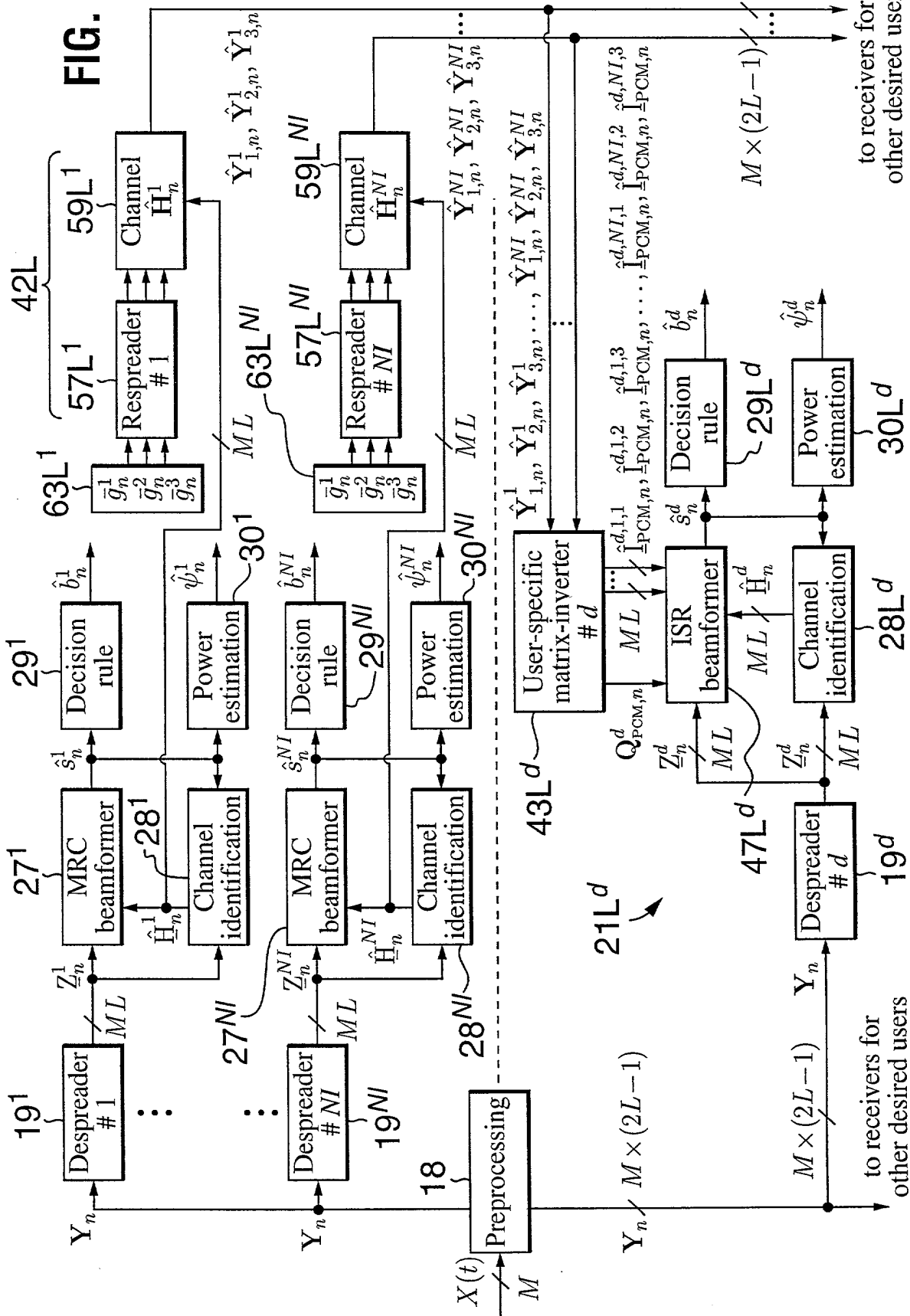


FIG. 24



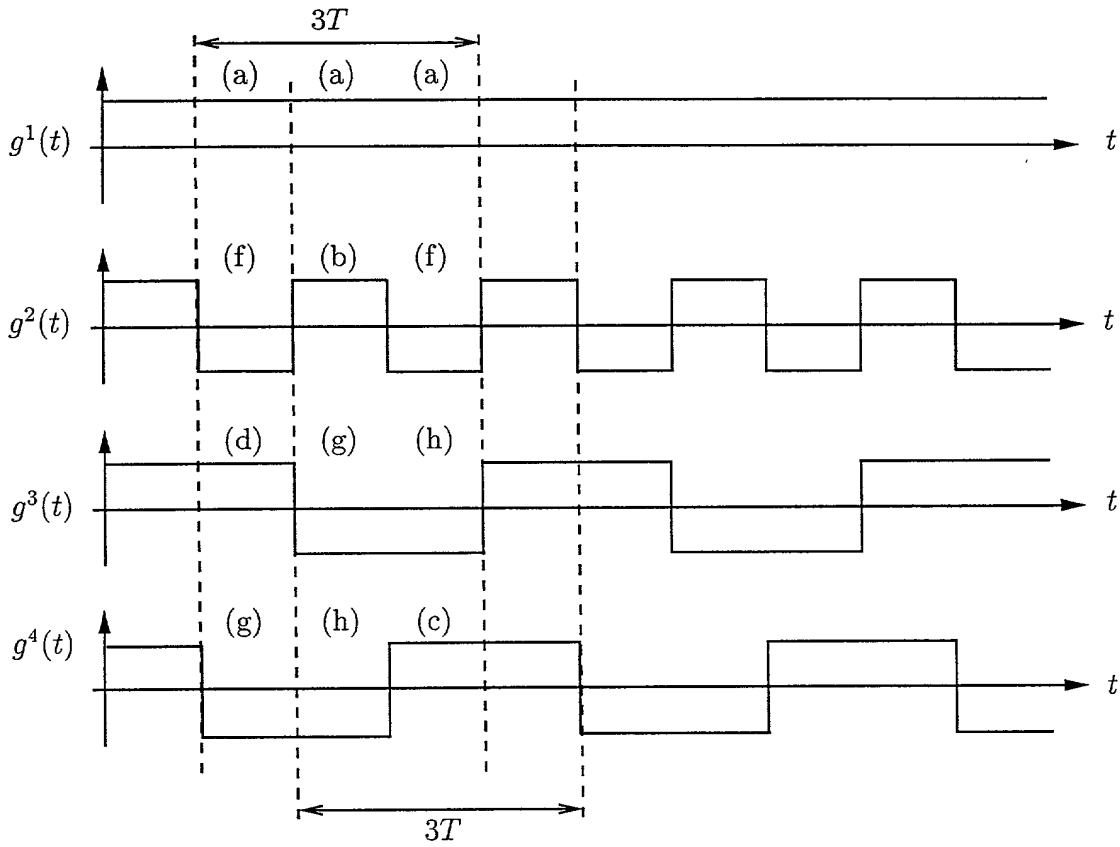
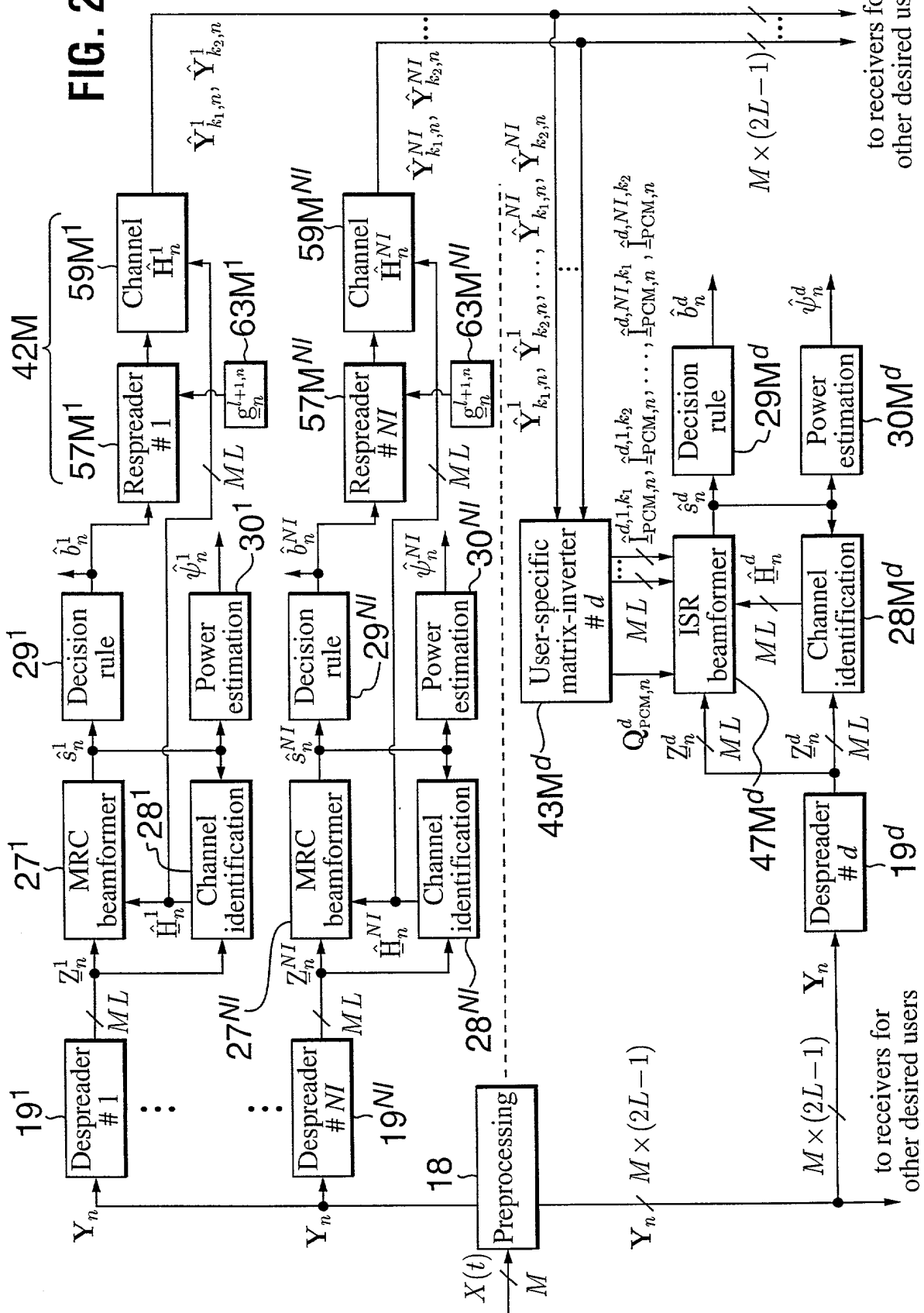


FIG. 25

FIG. 26



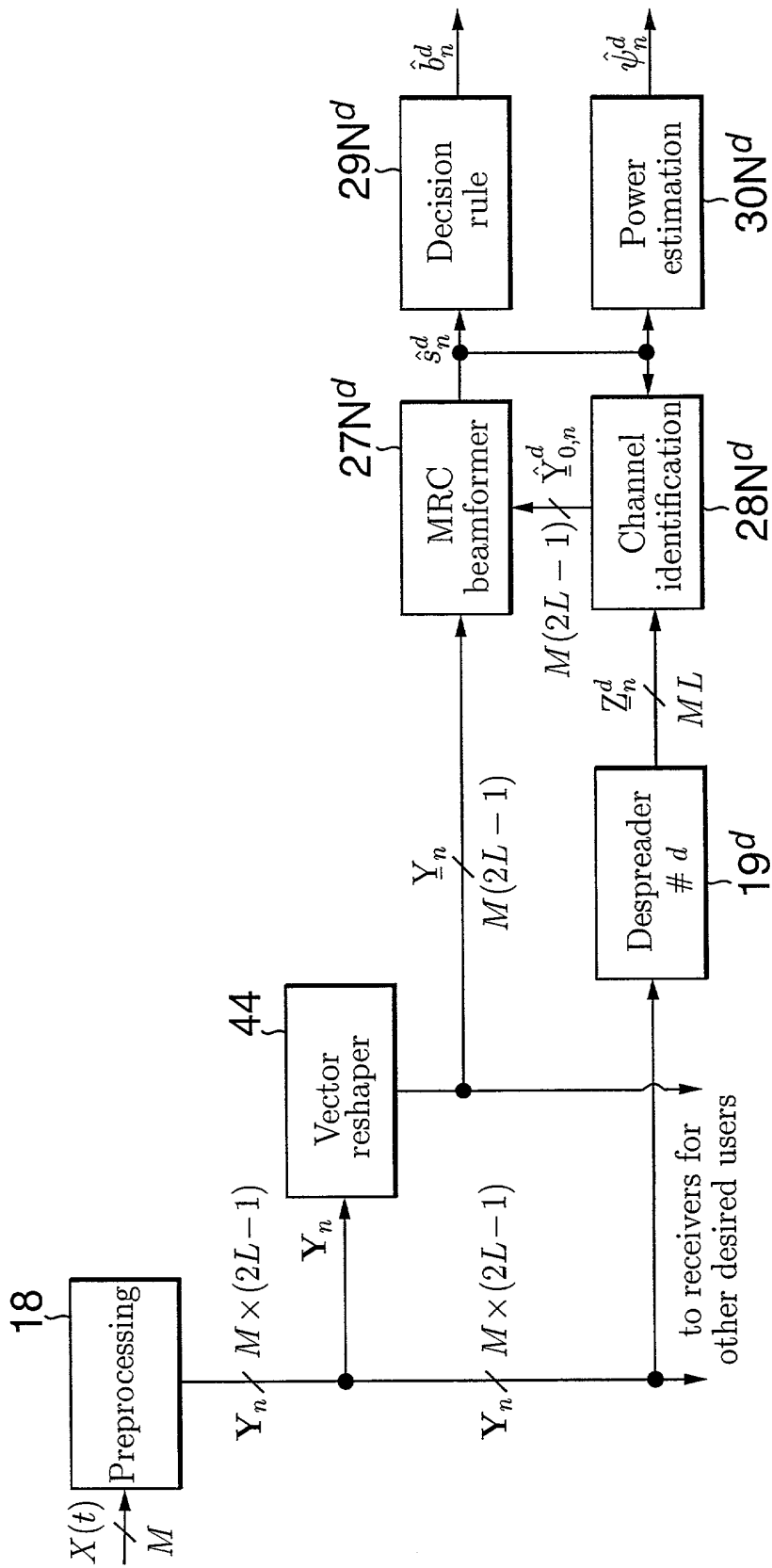
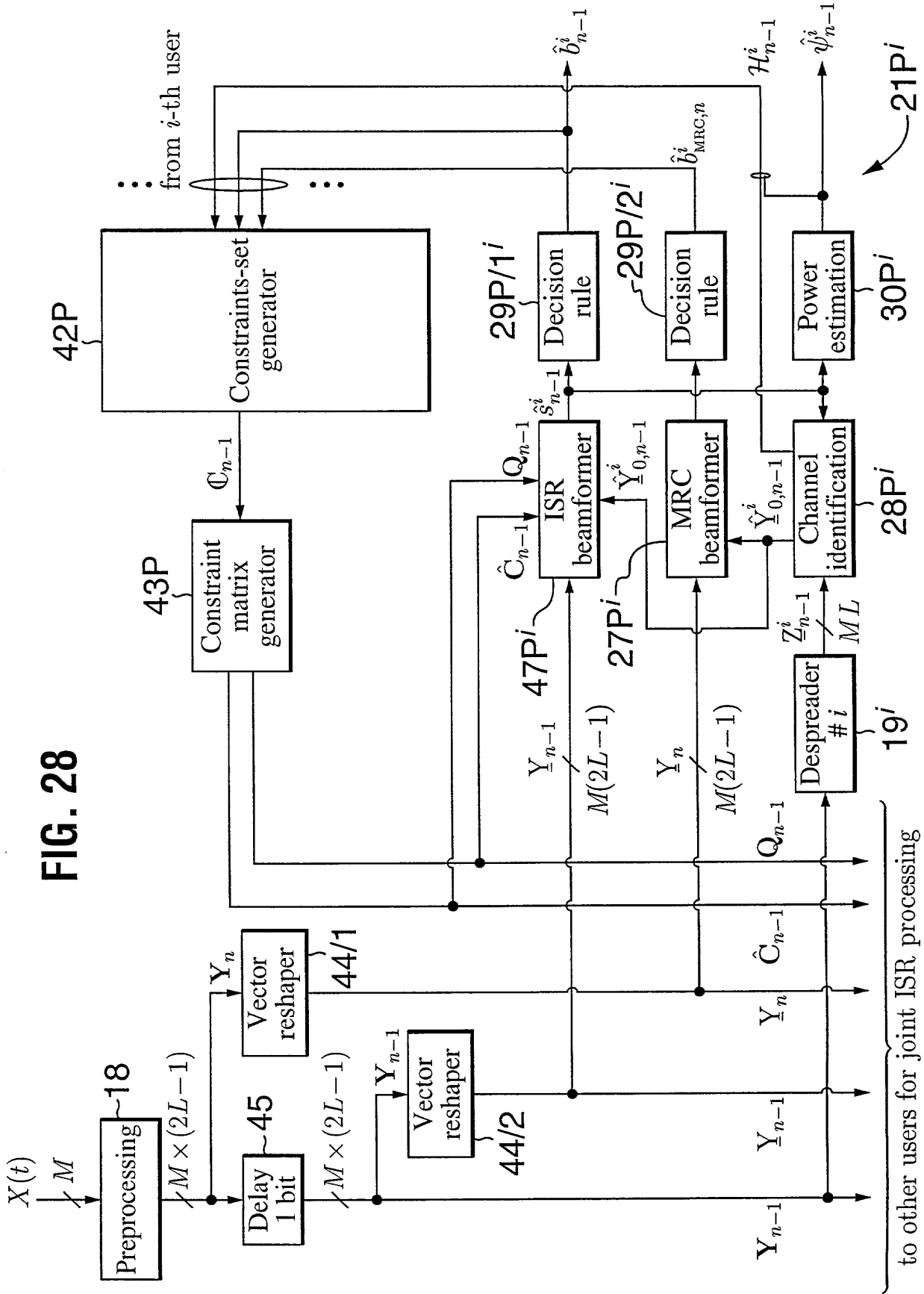


FIG. 27

FIG. 28



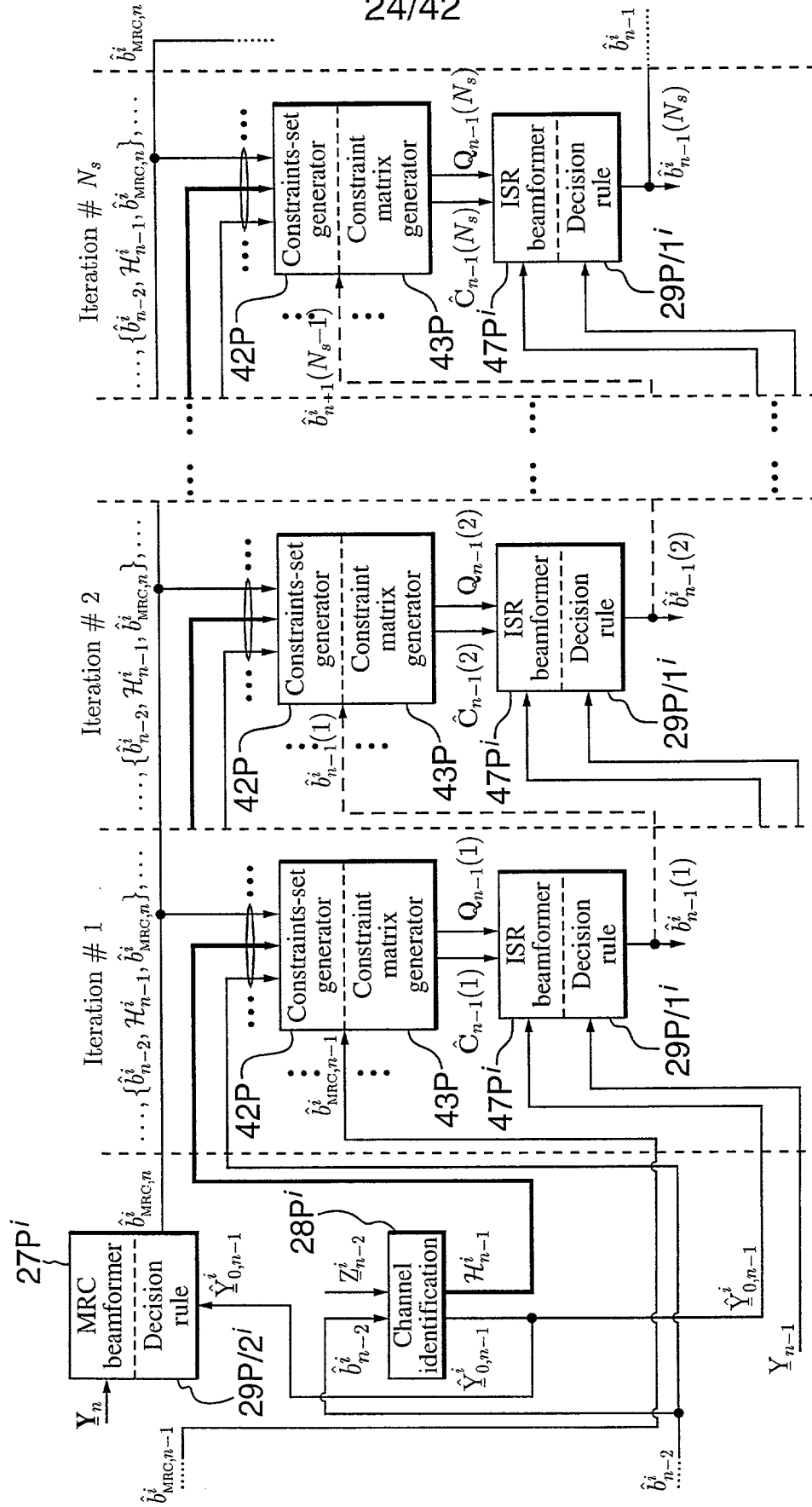
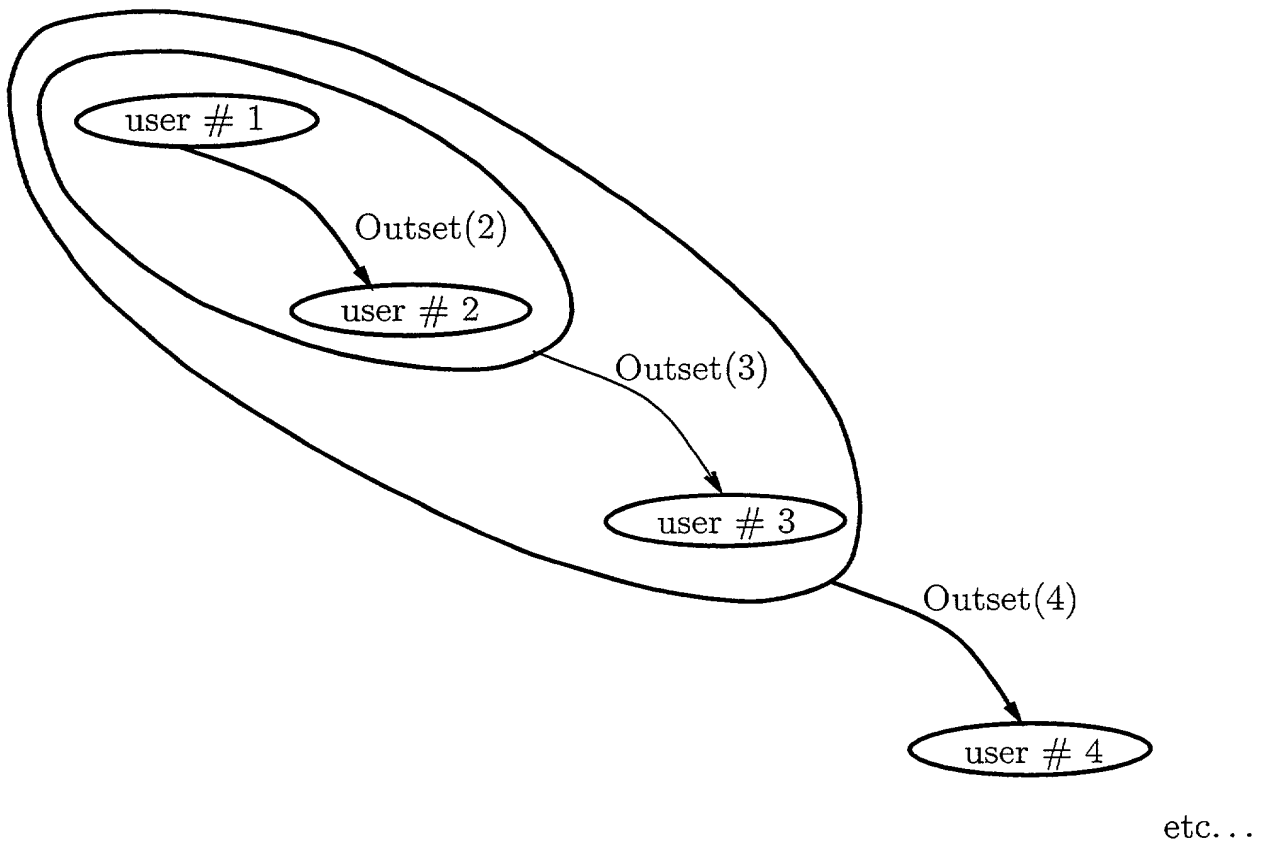


FIG. 29

**FIG. 30**

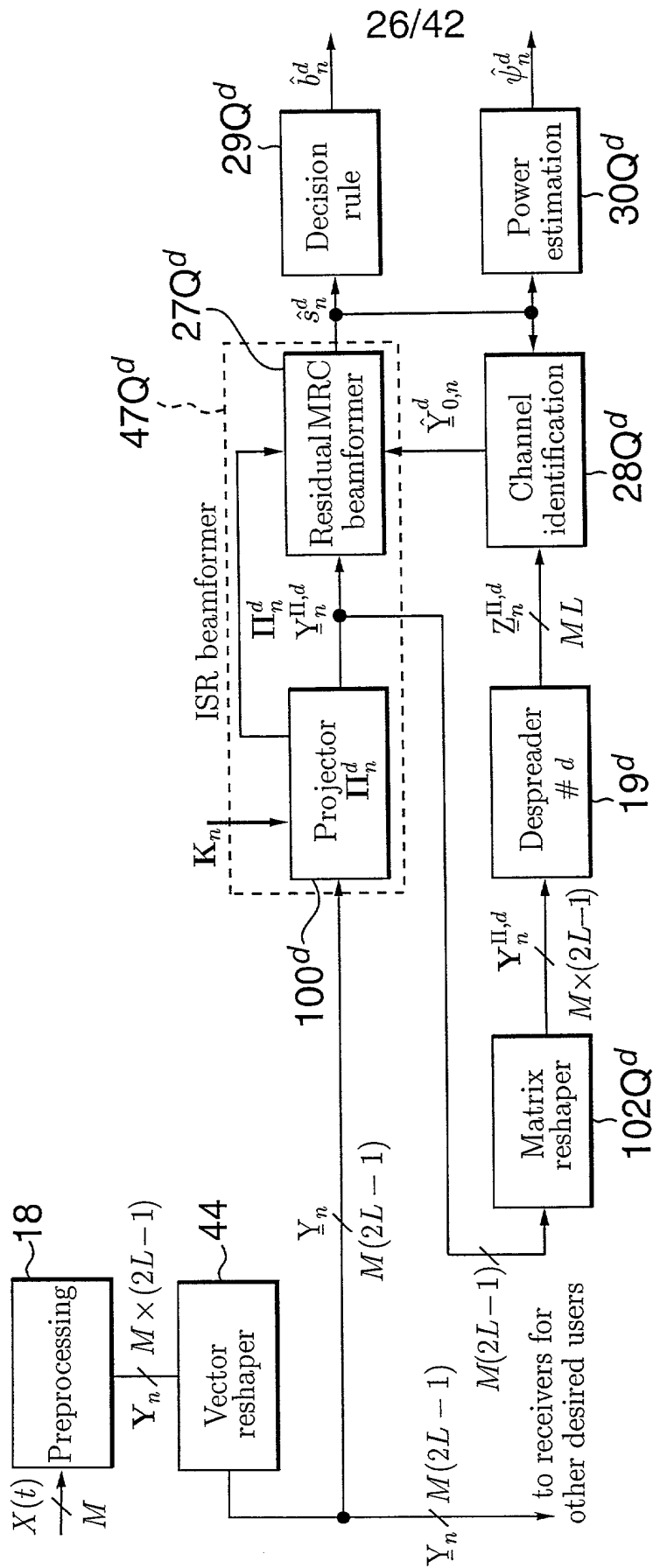


FIG. 31

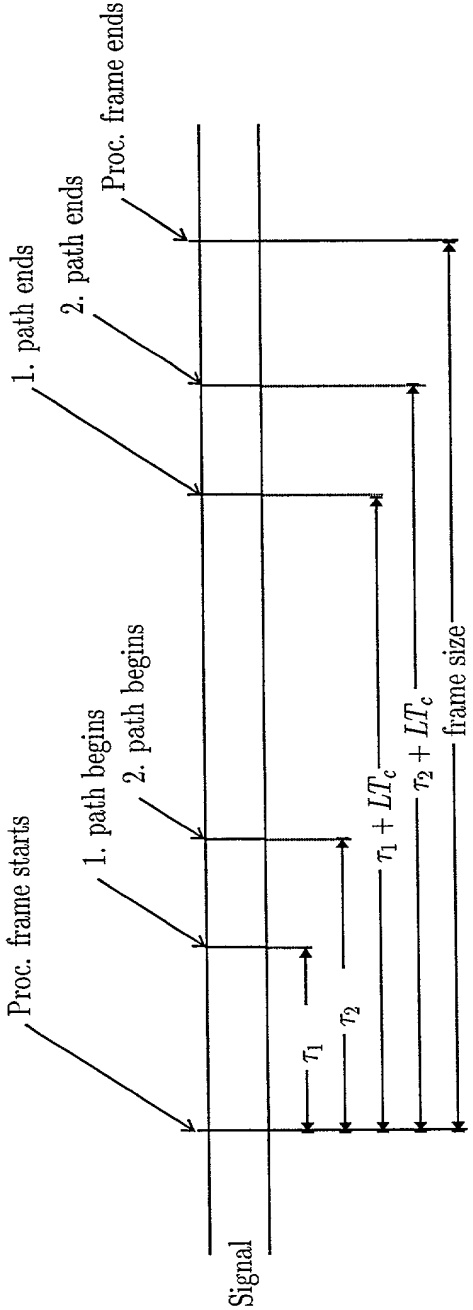


FIG. 32

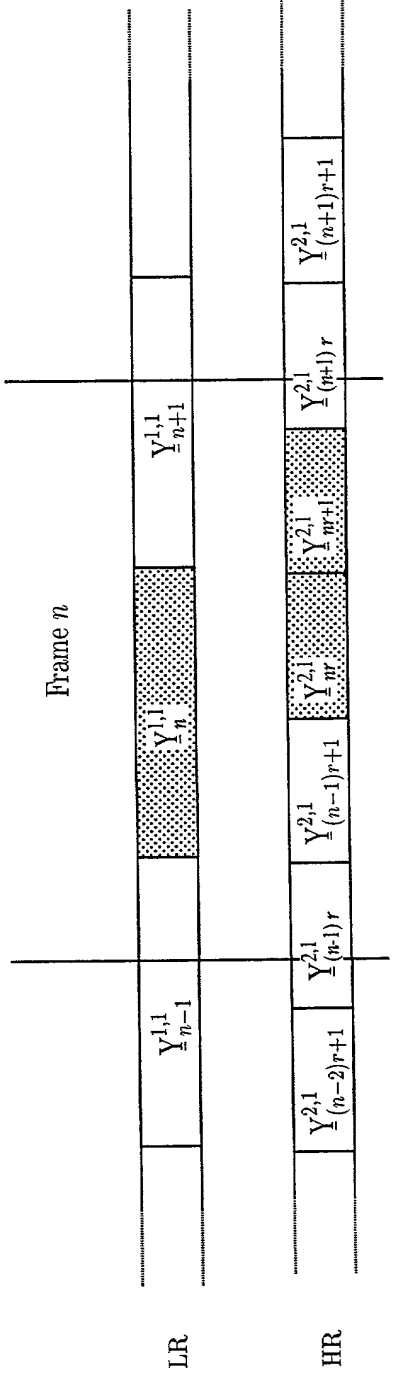


FIG. 33

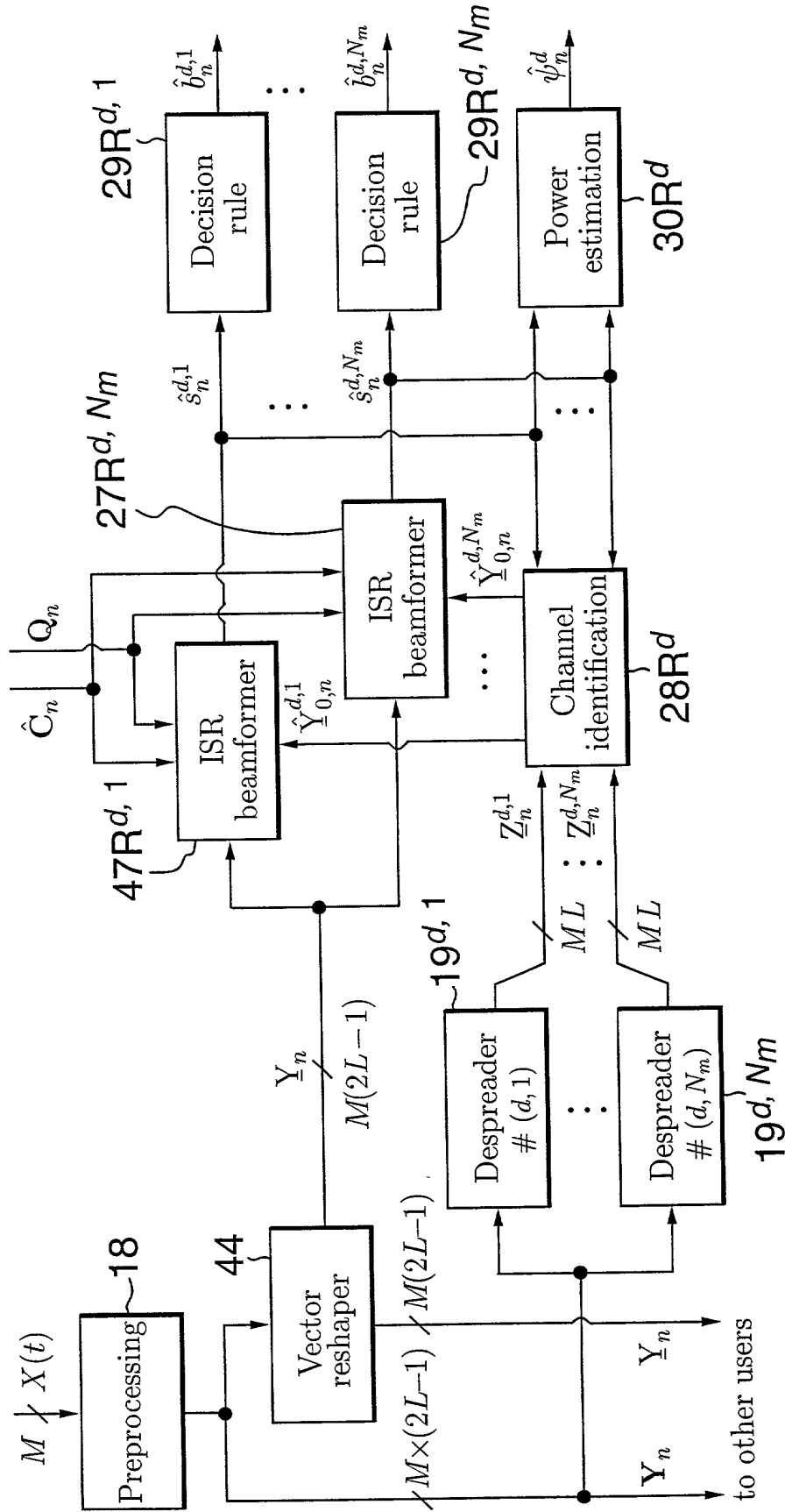


FIG. 34

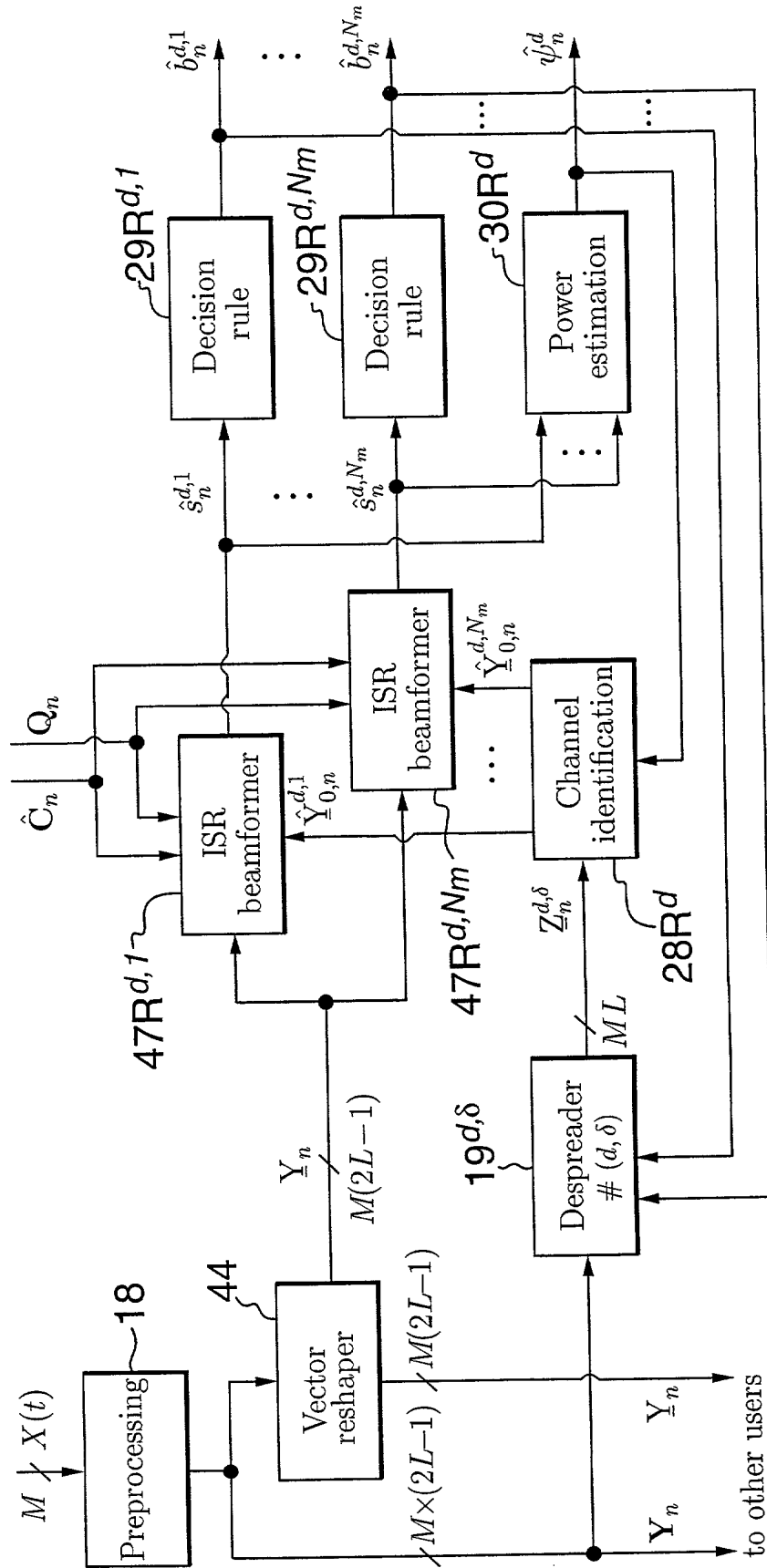


FIG. 35

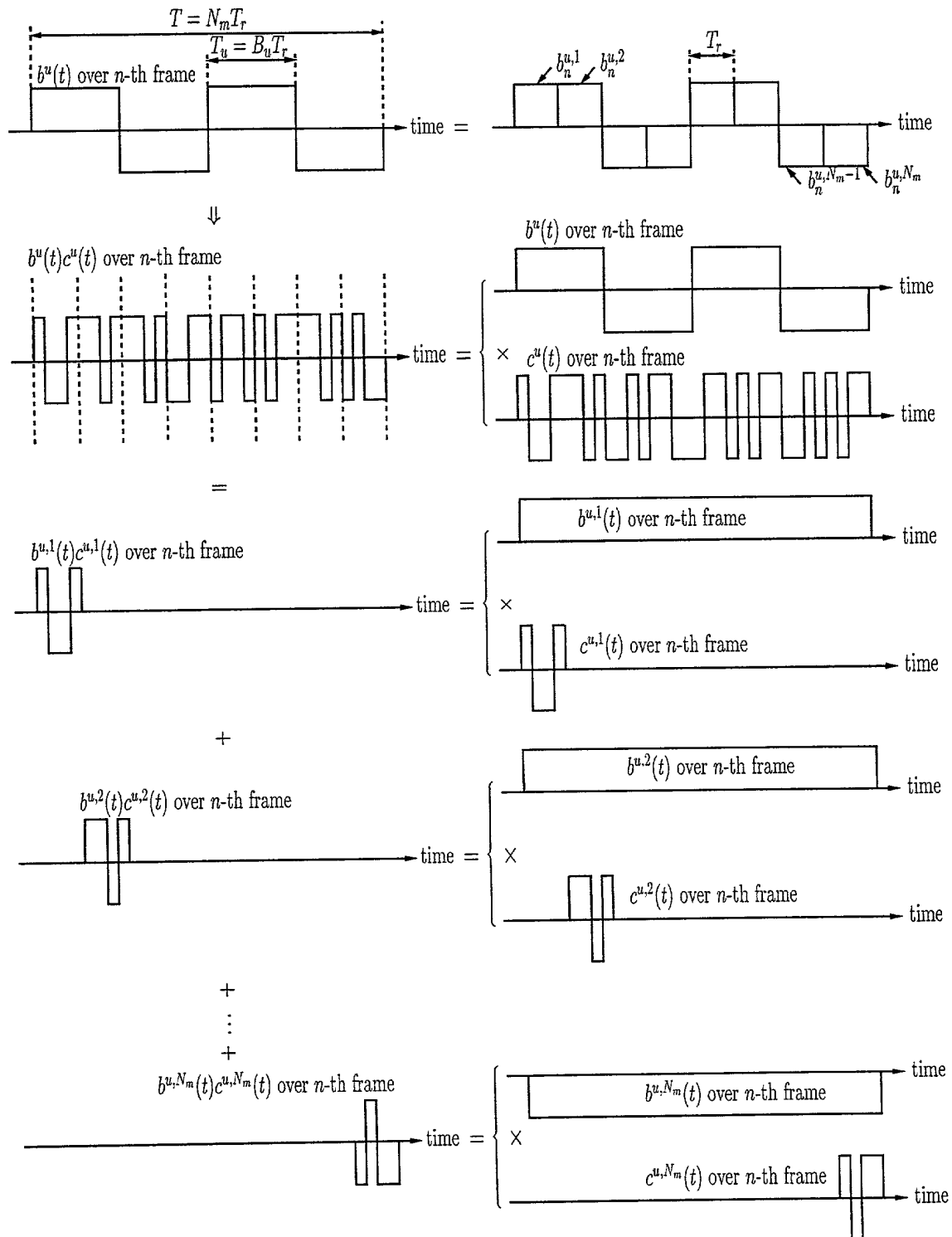


FIG. 36

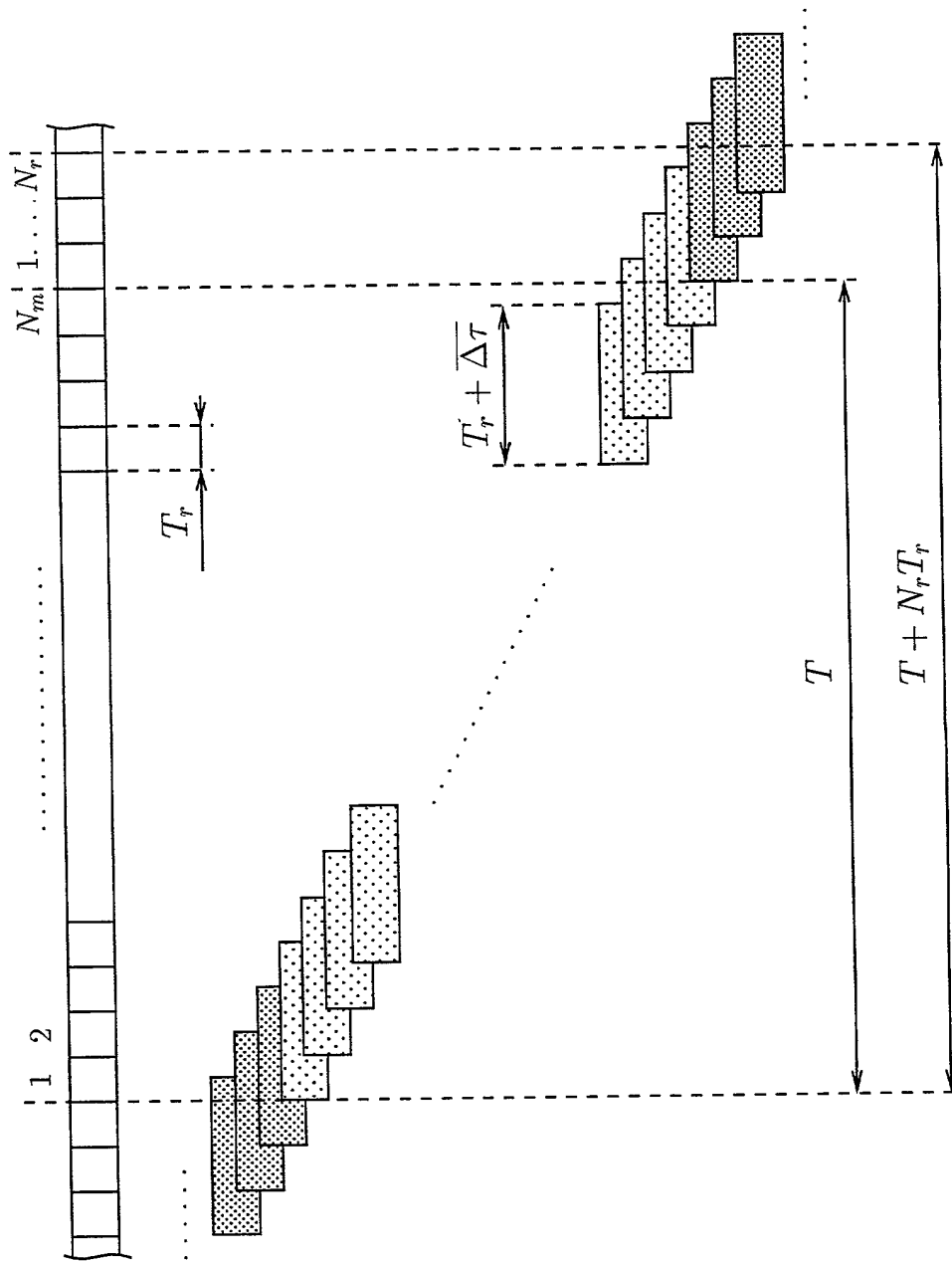


FIG. 37

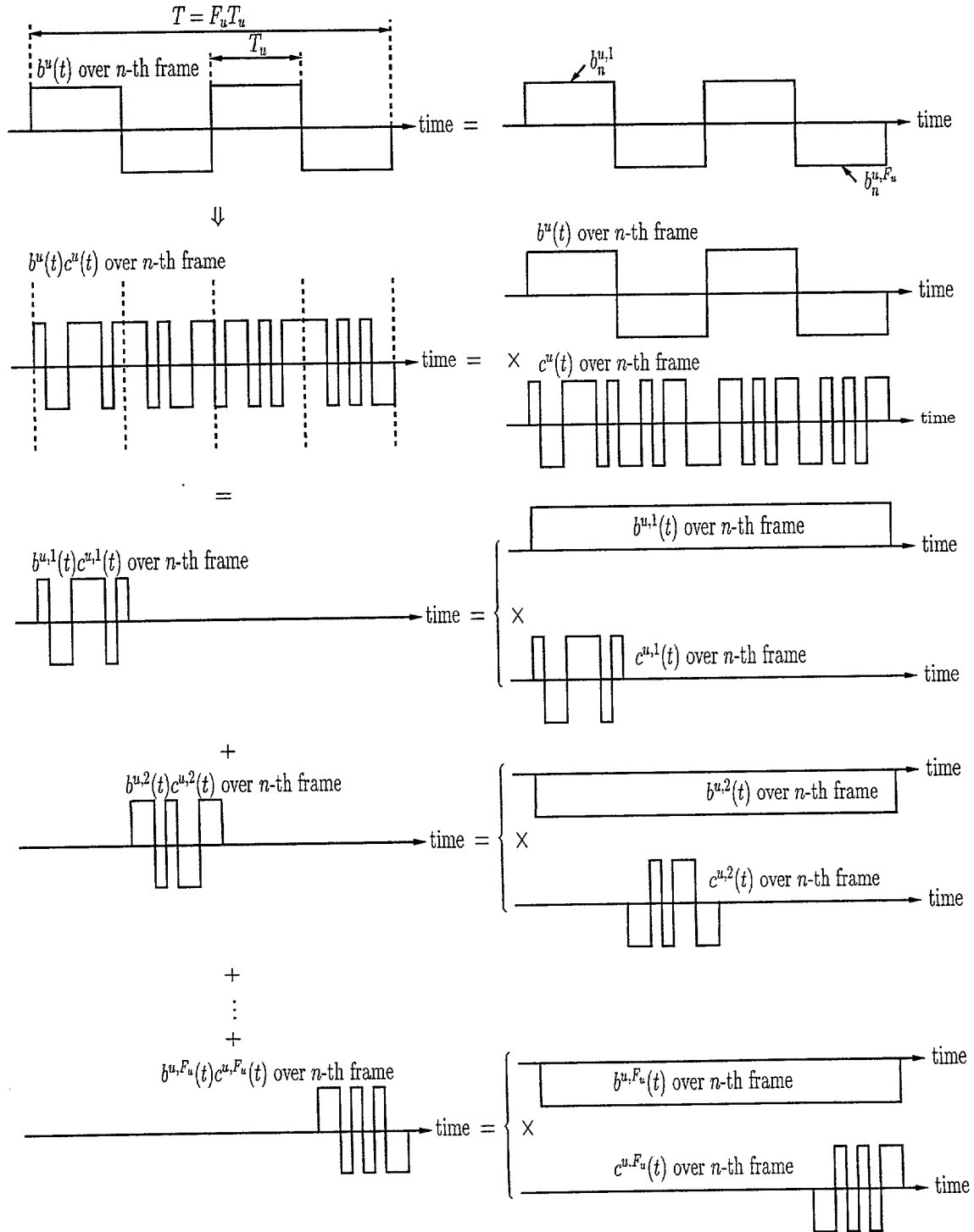


FIG. 38

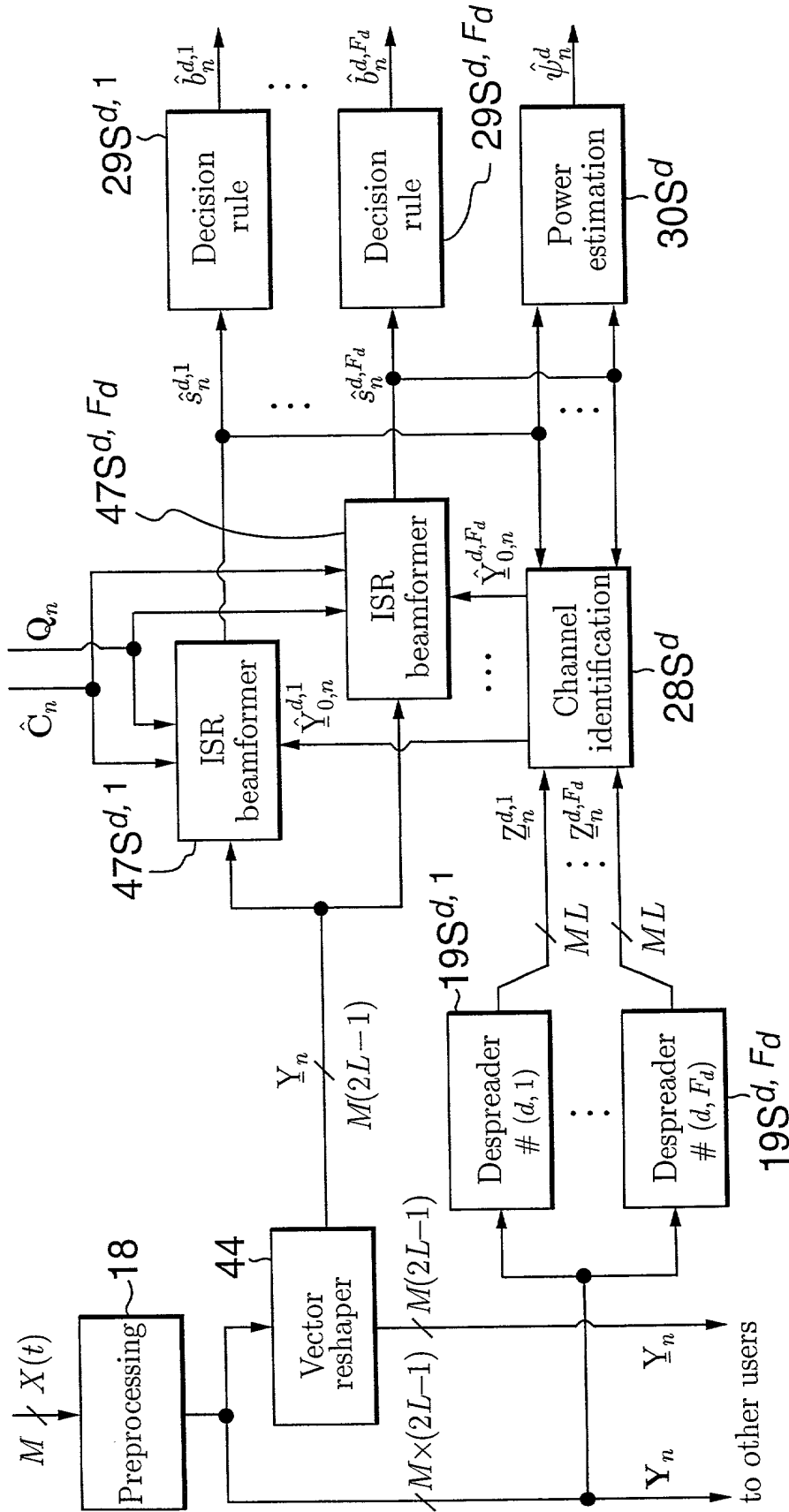


FIG. 39

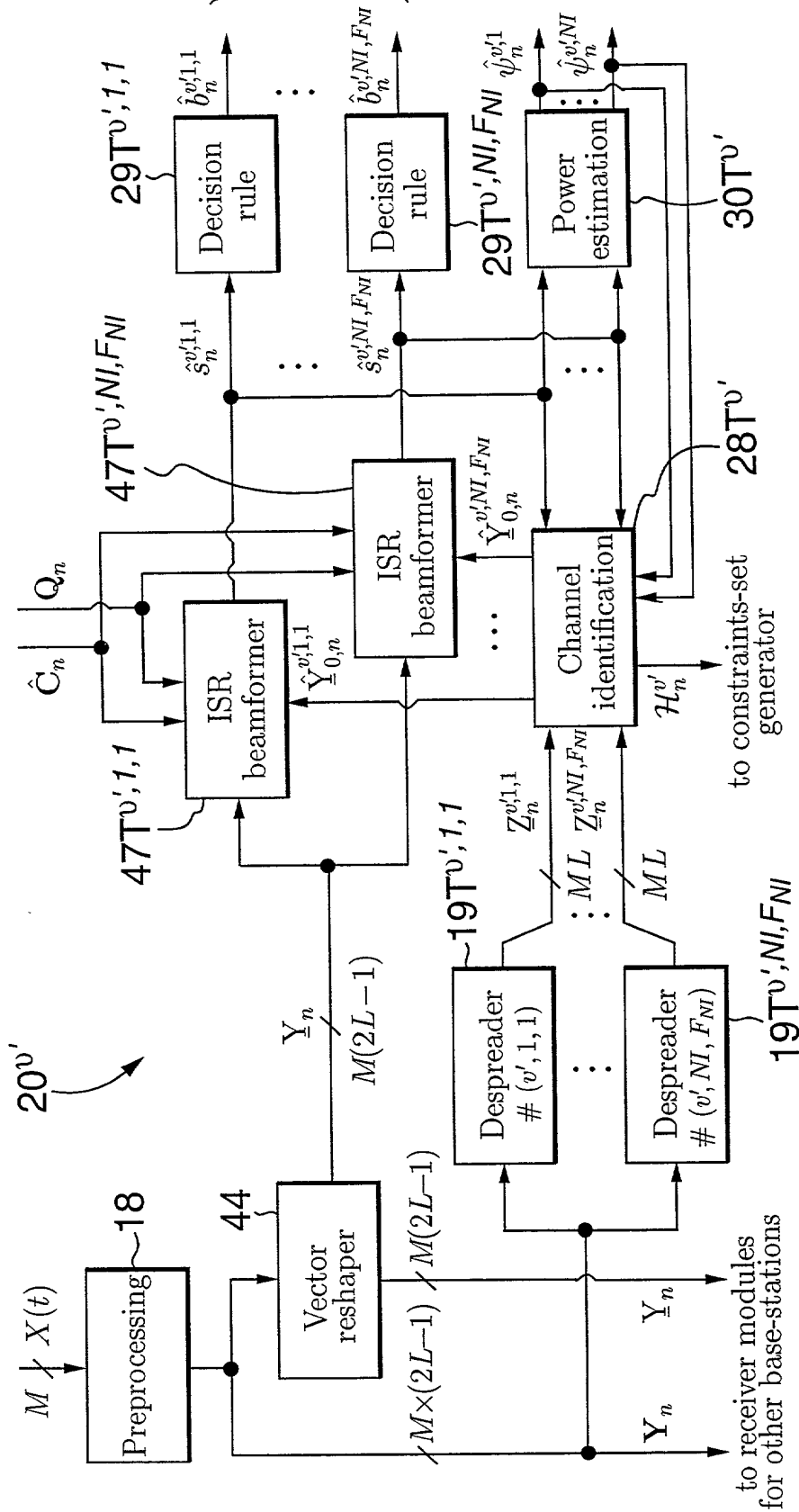


FIG. 40

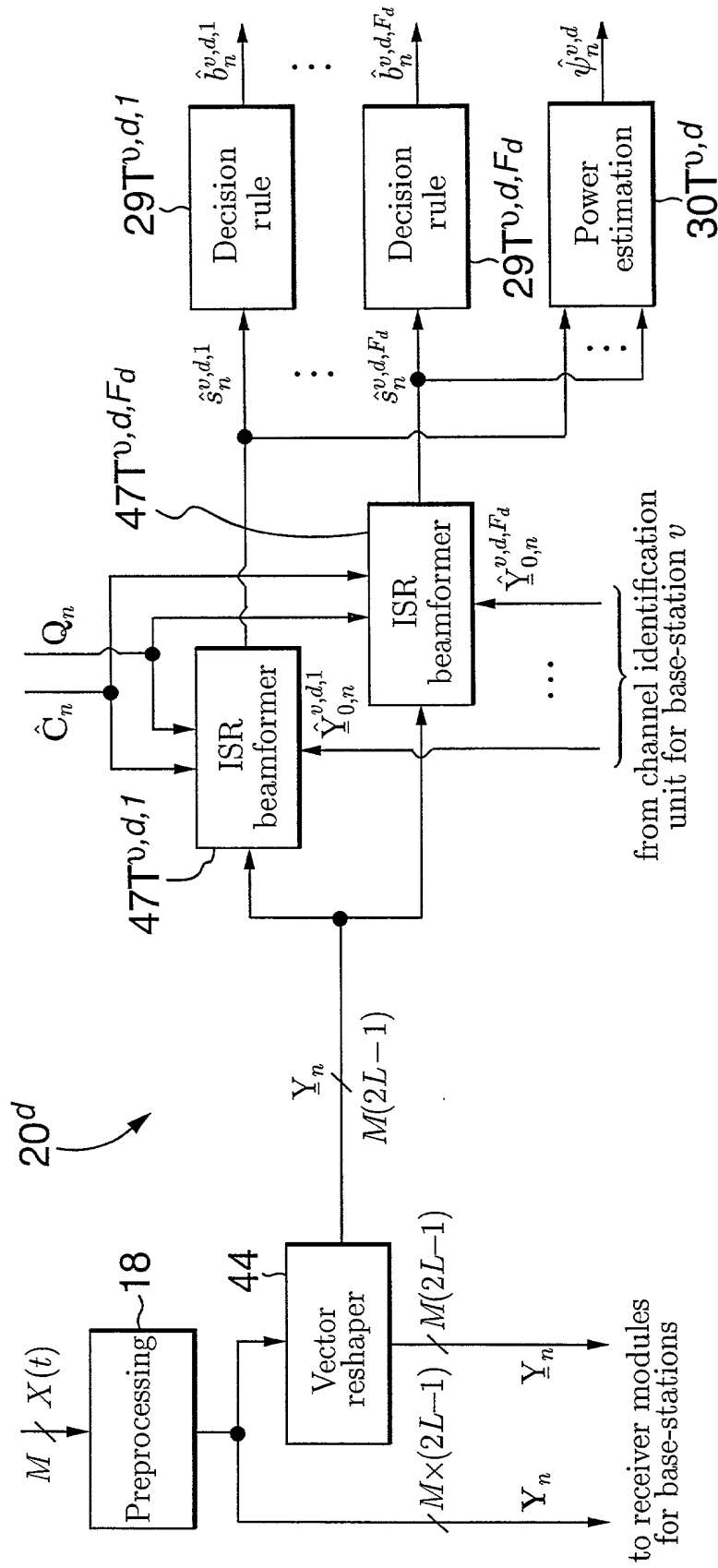


FIG. 41



FIG. 42

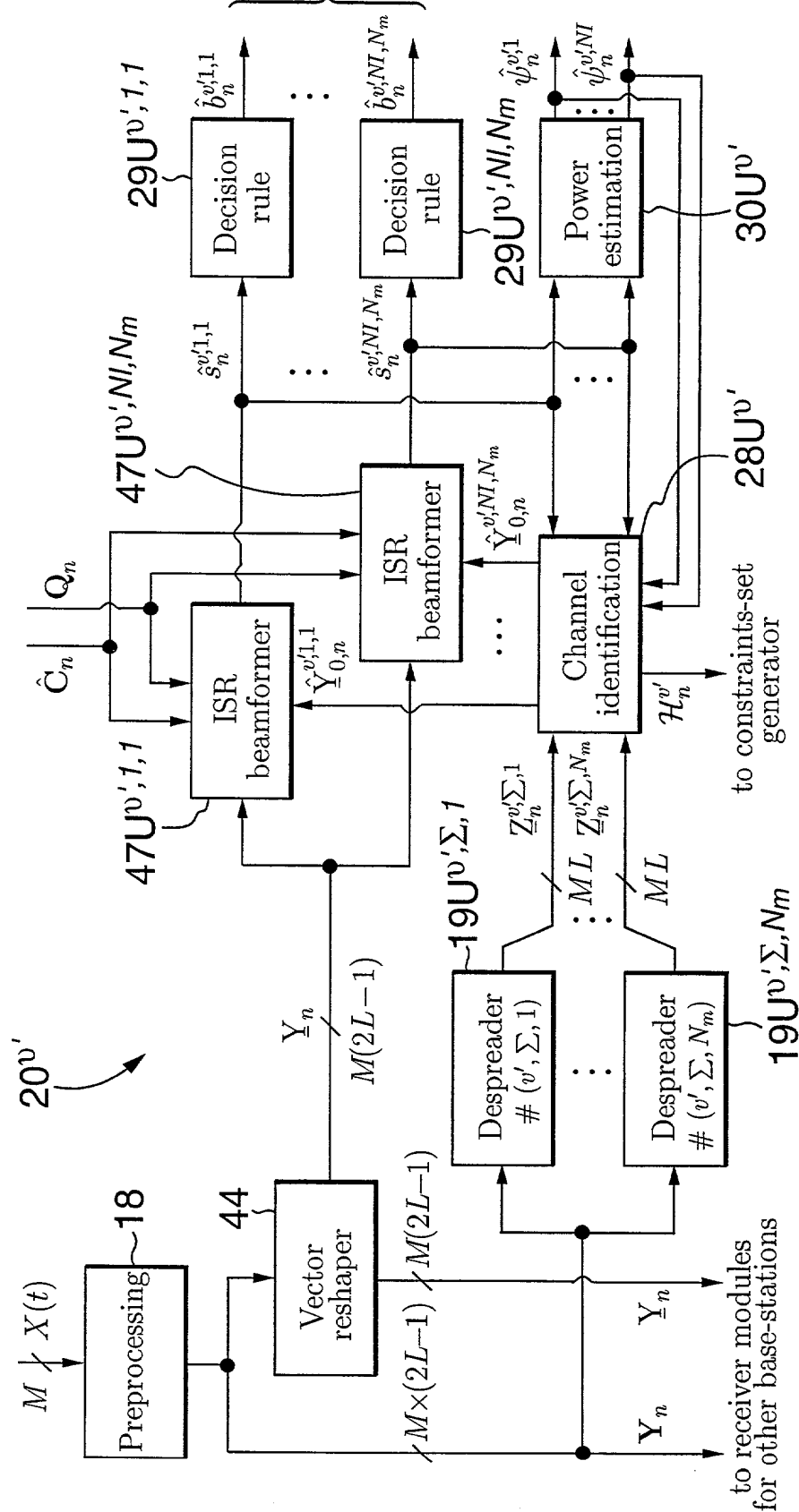
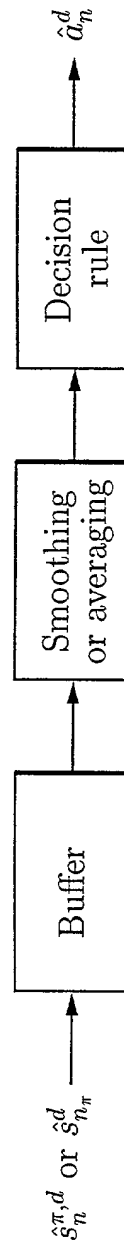
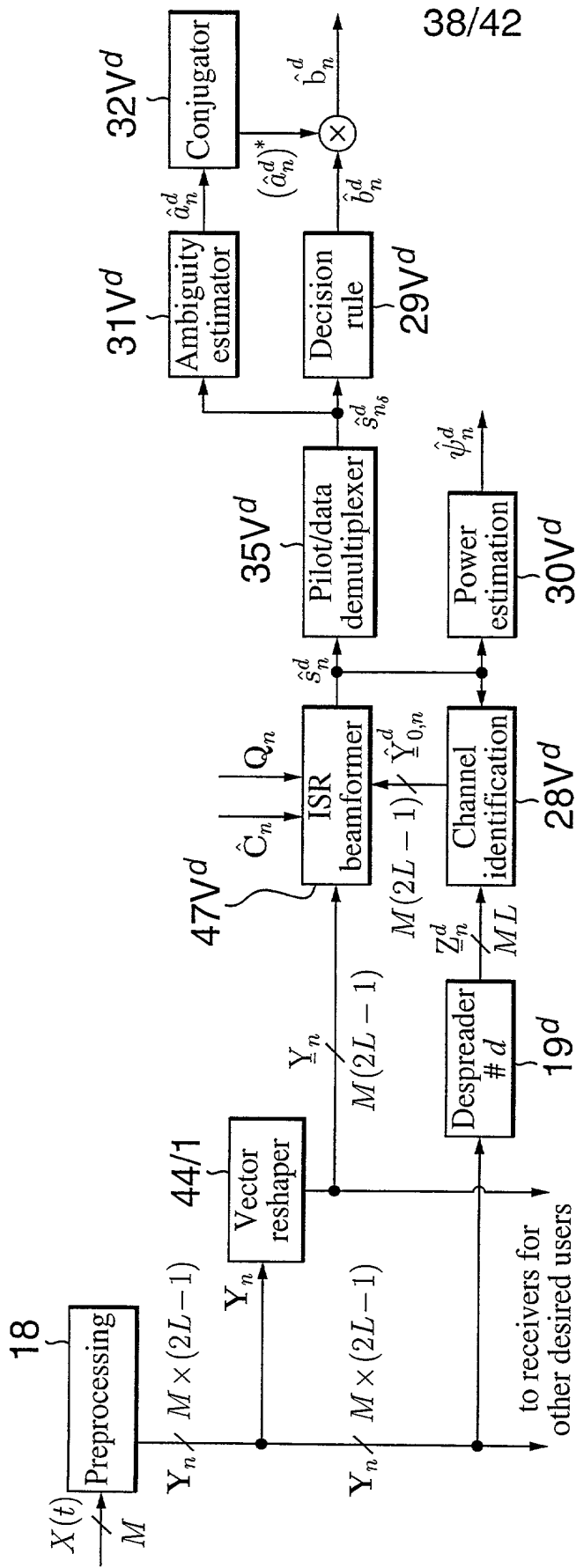


FIG. 43



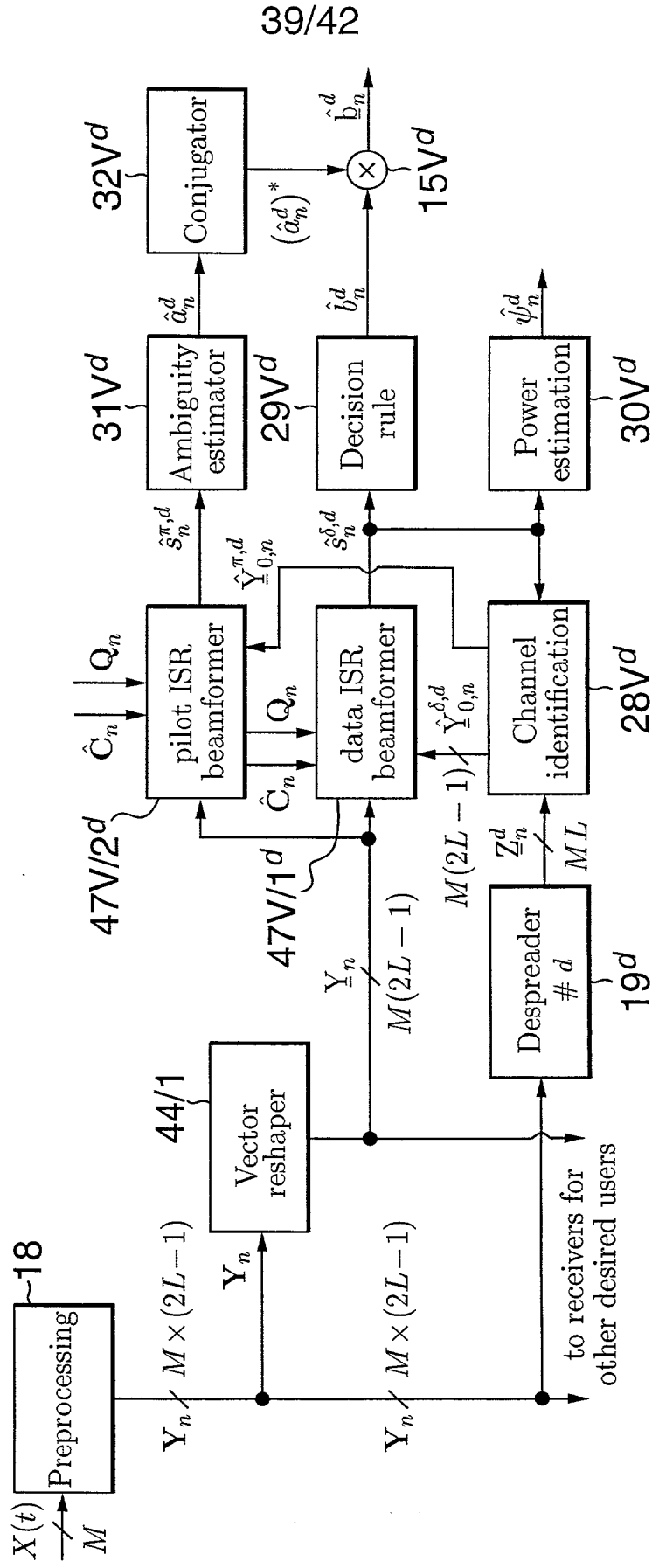


FIG. 46

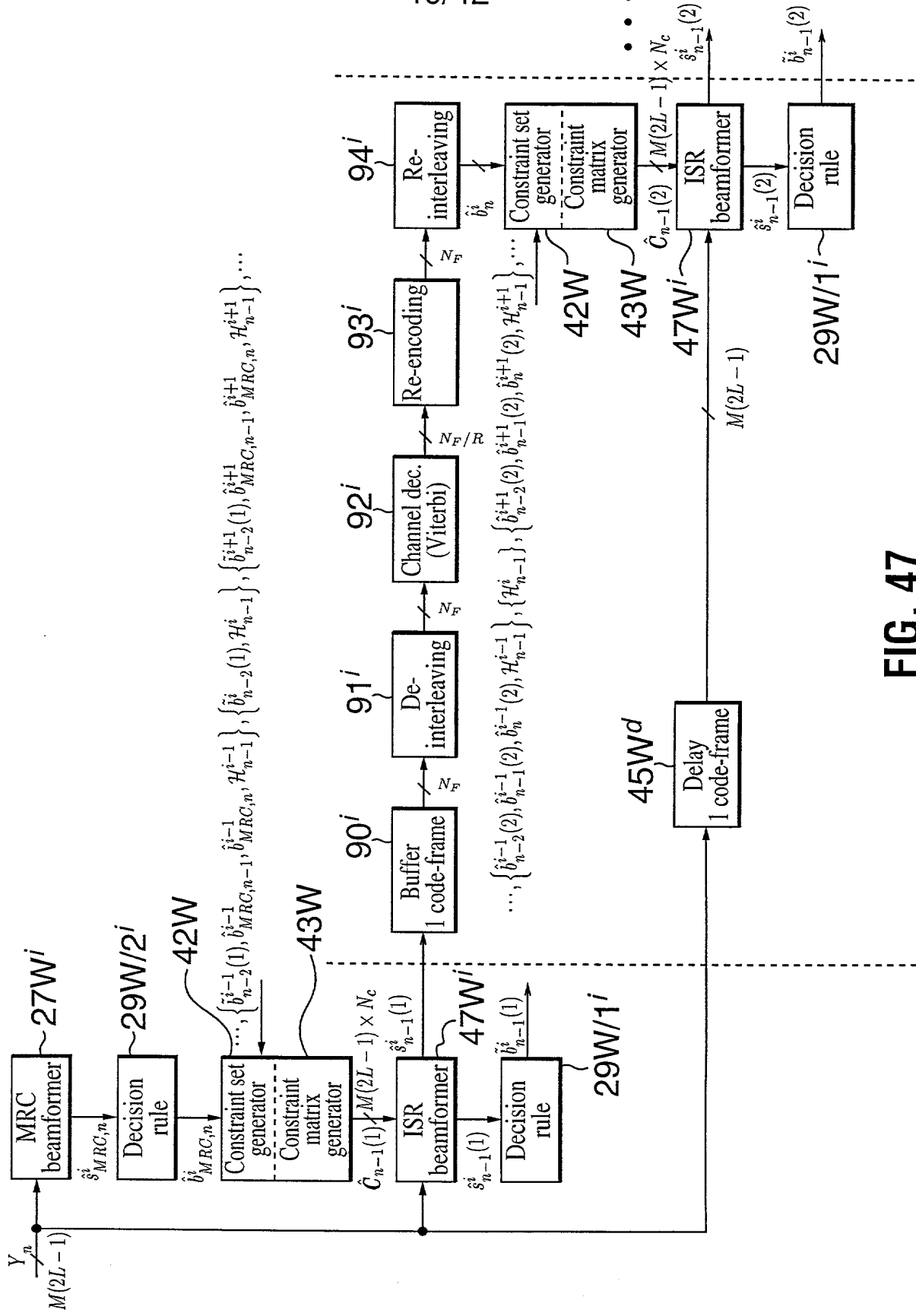


FIG. 47

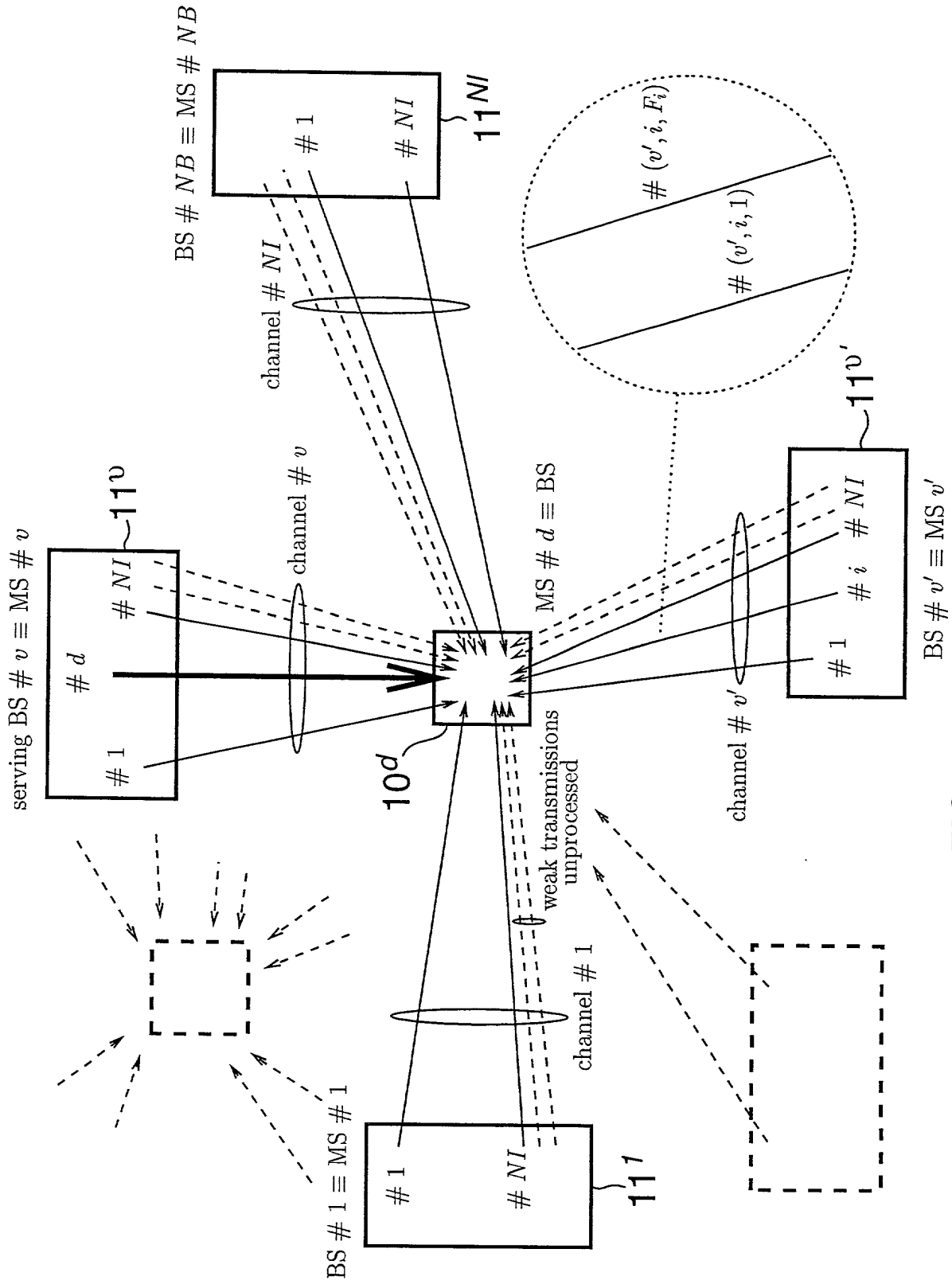


FIG. 48

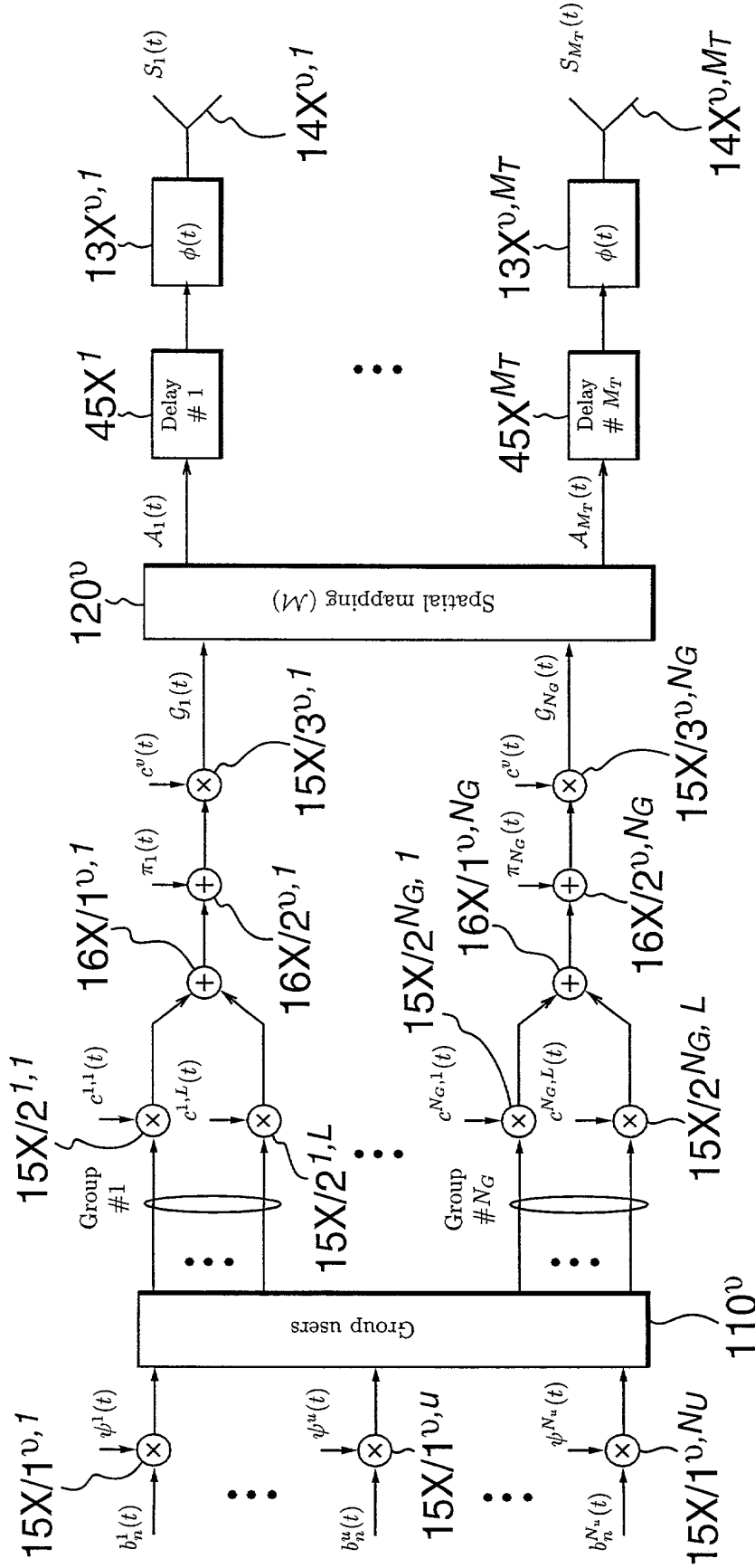


FIG. 49